AD NUMBER

AD802124

NEW LIMITATION CHANGE

TO

Approved for public release, distribution unlimited

FROM

Distribution authorized to U.S. Gov't. agencies and their contractors; Export Conrtol; Oct 1966. Other requests shall be referred to the Air Force Rome Air Development Center, Attn: EMLI, Griffiss AFB, NY 13440.

AUTHORITY

RADC, per USAE ltr dtd 17 Sep 1971

RADC-TR-66-505
Third Semi-annual Report

FAILURE MECHANISMS IN SEMICONDUCTOR DIODES

Byron L. Blair

General Electric Company

TECHNICAL REPORT NO. RADC-TR-66-505
October 1966

Rome Air Development Center
Research and Technology Division
Air Force Systems Command
Griffiss Air Force Base, New York

FAILURE MECHANISMS IN SEMICONDUCTOR DIODES

Byron L. Blair

General Electric Company

AFTC, GAFB, N.Y., 10 Nov 66-190

FOREWORD

This interim report was prepared by Byron L. Bair of General Electric Company, Semiconductor Products Department, Electronics Park; Syracuse, New York, under Contract AF30(602)-3624, project no. 5519, task no. 551906. RADC project engineer was John F. Carroll (EMERP).

Release of subject report to the general public is prohibited by the Strategic Trade Control Program, Mutual Defense Assistance Control List (revised 6 January 1965) published by the Department of State.

This report has been reviewed and is approved.

Approved: John F. Carroll
JOHN F. CARROLL
Reliability Physics Section
Reliability Branch

Approved: G.W. Wallace, MAJOR USAF
D. F. BARBER
Chief, Reliability Branch
Engineering Division

ABSTRACT

This is the third semi-annual report of a three year program to investigate those mechanisms which contribute to the long term degradation of diode parameters. This report is primarily concerned with the structuring, refining and verification of a Deterministic Model for diode failure. The Deterministic Model is presently separated into two portions; reverse bias degradation and forward bias degradation.

The reverse bias portion of the model was derived and discussed in the second Technical Documentary Report. This portion of the model is repeated in this report, which also contains :

- sample degradation rate constant calculations,
- a discussion of the preliminary verification of the model,
- the planned test matrix to complete the verification and refinement of the model,
- a summary of the failure analysis effort performed to structure and verify this portion of the model.

The forward bias portion of the model has proved to be more complex than the reverse bias portion. The observed response to stress has been multi-modal and dependent on the measurement bias voltages. This portion of the model is being structured, but the following points have been determined, and are discussed in this report:

- the temperature and pressure used in the sealing process have a major effect in the degradation response pattern,

- the degradation patterns following the sealing process, forward current stresses and at very high temperature stress at zero bias are identical,
- the degraded devices, which had been stressed in the sealing process, exhibited microplasma light emission, low amplitude microplasma noise pulses and reverse voltage walkout,
- the observed failure mechanisms seem to be surface, rather than bulk, related phenomena.

There is evidence to indicate that the model should be based on the high temperature decomposition of a compound into components, at least one of which is active in increasing the surface electron concentration. The planned test matrix to complete the structuring, verification, and refinement of the model has been designed and is discussed in the report. In addition, a summary of the failure analysis effort performed to date on this portion of the model is included. Failure analysis will become an even more important part of the work effort to achieve the objectives of the program. This report contains an explanation of the physical nature of the failure mechanisms and a complete Failure Mode Chart which defines failure codes and relates the failure mode categories, failure mechanisms and failure causes.

The comprehensive step-stress tests have been continued. The 175°C forward current, forward voltage and reverse voltage stresses are completed, and the data analysis will be included in the next report. The 200°C and 225°C stresses will be completed next. The step-stress data will be used to extend the range of the reverse bias portion of the Deterministic Model as well as to make certain that all the necessary stresses are included in the Deterministic Model test plan.

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

SECTION I

DIODE DEGRADATION STUDIES

1.1 Introduction

The work of the current reporting period was concentrated on the degradation which followed forward bias stressing. It was found that there were other characteristic features of the degraded diodes in addition to the excess reverse current. Degradation patterns, similar to those resulting from forward bias stress, were also found to be caused by some other types of stress. The sealing process, which subjects the pellet to high temperature and pressure, leads to a degradation of the diode characteristics quantitatively similar to that resulting from forward current stresses. The degradation is relieved by an annealing and heat aging process, although some of the degradation remains in some of the units. Pellets which were studied before the sealing process were found to be very stable against forward current degradation. Storing diodes without bias at high temperature was also found to degrade the diodes in the same manner as the forward current. The characteristic responses to these stresses were:

1. excess reverse current
2. walkout
3. microplasma light emission
4. microplasma noise.

Observation of microplasma light and noise suggested a model of the failure mode based on ion motion in or near the silicon-silicon oxide transition region which caused a decrease in the surface breakdown volt-

rge. The excess current was determined to be the superposition of the currents of many localized breakdown regions.

1.2 The Nature of the Forward Bias Degradation

The following paragraphs describe the degradation response of the diode following the application of large forward currents. Figure 1 shows a log-log plot of representative voltage-current characteristics for currents less than one milliampere. For currents greater than one milliampere, the forward current increased less rapidly with forward voltage, and at 100 milliamperes, the mean forward voltage drop was 0.97 volts. The primary degradation caused by forward current stressing was an increase of the reverse current as measured at room temperature. The five important variables which determined the change in reverse leakage current were:

I_F - The forward current at which the diode was stressed.

T - The ambient stress temperature.

t_S - The duration of the stress.

V_R - The reverse voltage at which the current was measured.

T_M - The measuring temperature.

No significant changes in the forward characteristic, or in the reverse characteristic below 100 millivolts, have been observed to result from these stresses. To emphasize diode to diode variance, Figure 2 shows a linear plot of the reverse voltage-current characteristic for three diodes from the same diffusion lot. Probing the reverse characteristics of pellets which were not sealed showed:

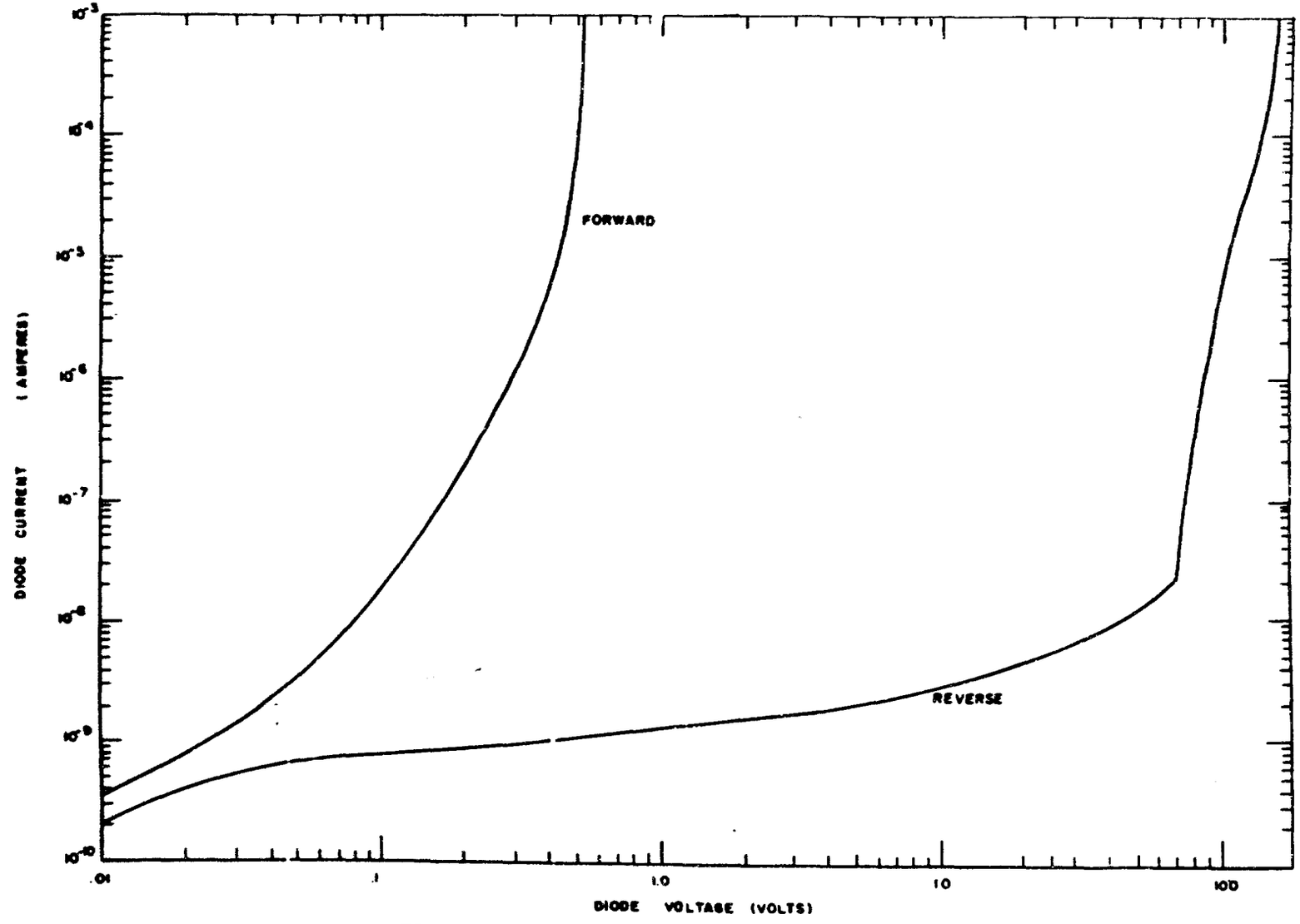


FIGURE 1

REPRESENTATIVE VOLTAGE- CURRENT CHARACTERISTICS

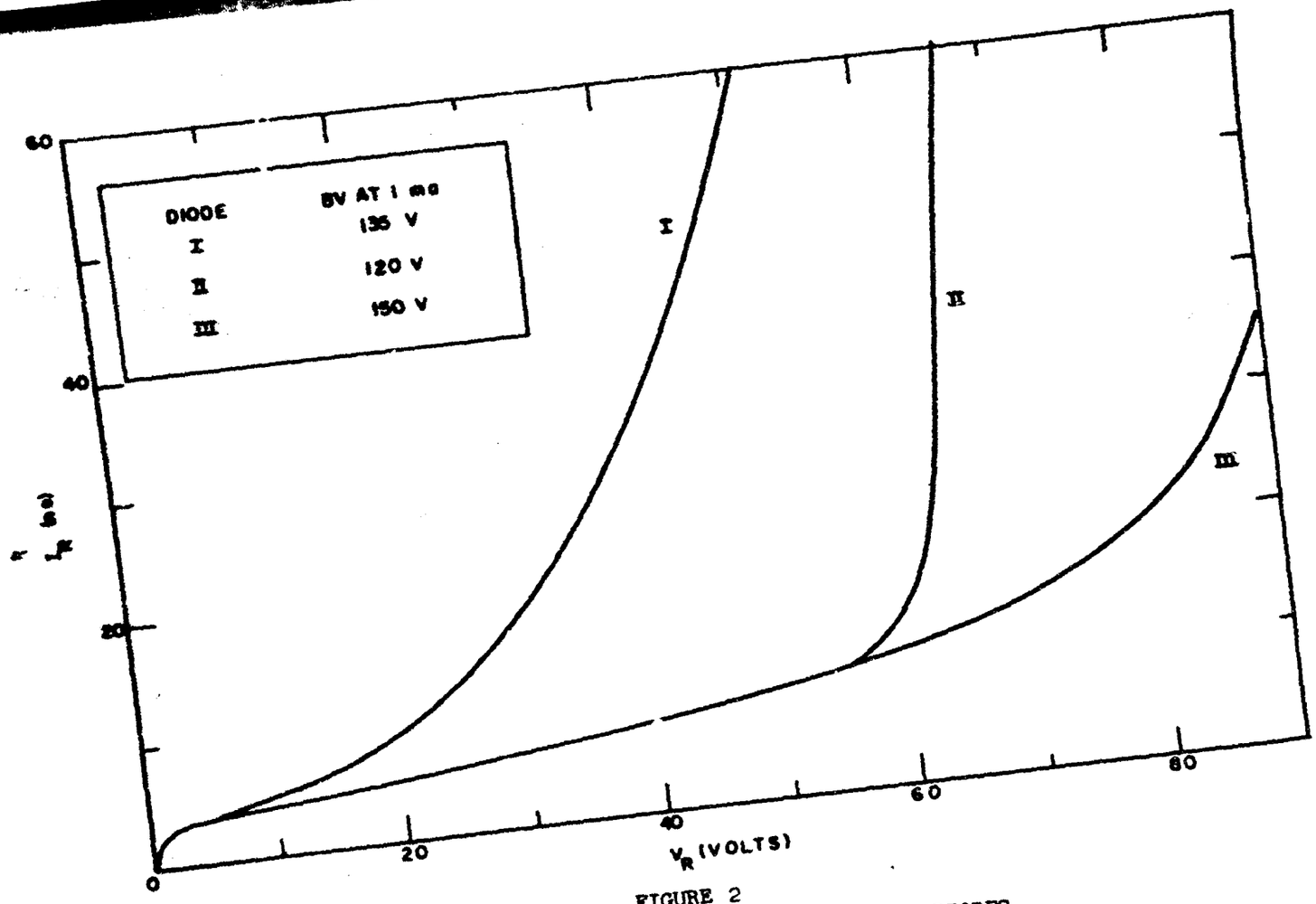


FIGURE 2

REVERSE CHARACTERISTICS OF THREE DIODES

1. a lower average current in the range from 30-80 volts
2. less variation from unit to unit.

As discussed below, the significance of this observation to the reliability studies was that the pellets which were not fabricated into finished devices were far less susceptible to the forward bias degradation. Moreover, the fabrication process was known to lead to a mode of device degradation which had many characteristics identical to those resulting from forward bias stressing; that is, the fabrication process caused the diodes to exhibit large reverse leakage currents, walkout, microplasma noise, and light emission. Thus, the individual differences among diodes shown in Figure 2 were the result of differing levels of degradation resulting from the sealing process and differing amounts of recovery during the aging and annealing process. These effects will be monitored in the deterministic model test plan, which is discussed later. It did not appear, however, that the remnant damage following the aging process provided a basis for screening the diodes for susceptibility to forward bias degradation. However, successful screening procedures have been demonstrated and will be discussed later.

Figure 3 illustrates a response which was shown by roughly one-third of the diodes tested. The solid lines show the state (measured at room temperature) of the diode after various periods of stress at forward currents of 200 milliamperes and an ambient temperature of 180°C. The characteristics were recorded with an X-Y recorder after each period of stress. The solid lines indicate the progressive nature of the degradation and show that, unlike the reverse bias mode, there was no indication of

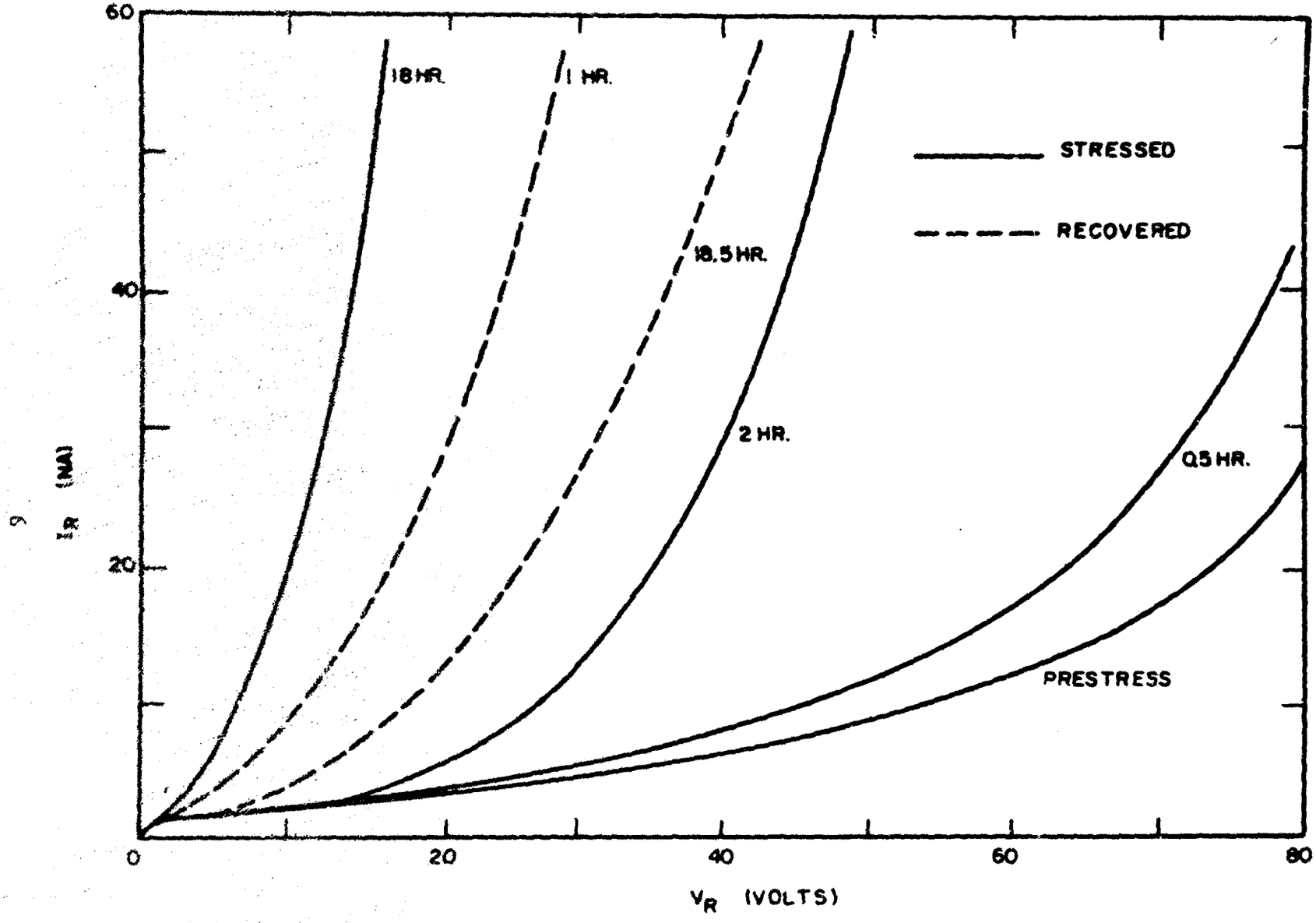


FIGURE 3

POWER LAW DEGRADATION

any saturation of the degradation after long periods of stress. The results of annealing the units at 440°C without an applied bias are shown in the dashed curves. It is seen that there was a rapid initial recovery, but after 18 hours the recovery was far from complete. In less severely degraded diodes, nearly complete recovery resulted from the annealing process. Temperatures in the 500°C to 600°C range resulted in recovery at low voltages, but increased degradation at higher voltages. Some of the diodes were found to degrade rather than recover under zero bias annealing. The dependence on reverse measuring voltage was also different from that of the reverse bias failure in that the excess current increased rapidly with reverse voltage. Figure 4 is a log-log plot of the excess current as a function of reverse voltage, and the slope indicates that below approximately forty volts δI_R was proportional to V_R^n with n values in the range from two to four.

Larger exponents were necessary to fit the excess current at large voltages in the heavily degraded devices. The fact that different exponents were needed to fit the excess current curves when the diode had experienced different amounts of stress indicated that the power law behavior of the excess current was not fundamental to the failure mechanism being investigated. However, to distinguish this type of degradation from that shown in Figure 5, it is convenient to use the term power law degradation for the behavior shown in Figures 3 and 4.

Figure 5 shows another form of reverse current degradation frequently observed after forward bias stressing. There was no excess current until a certain critical voltage was applied. Above this voltage, the current

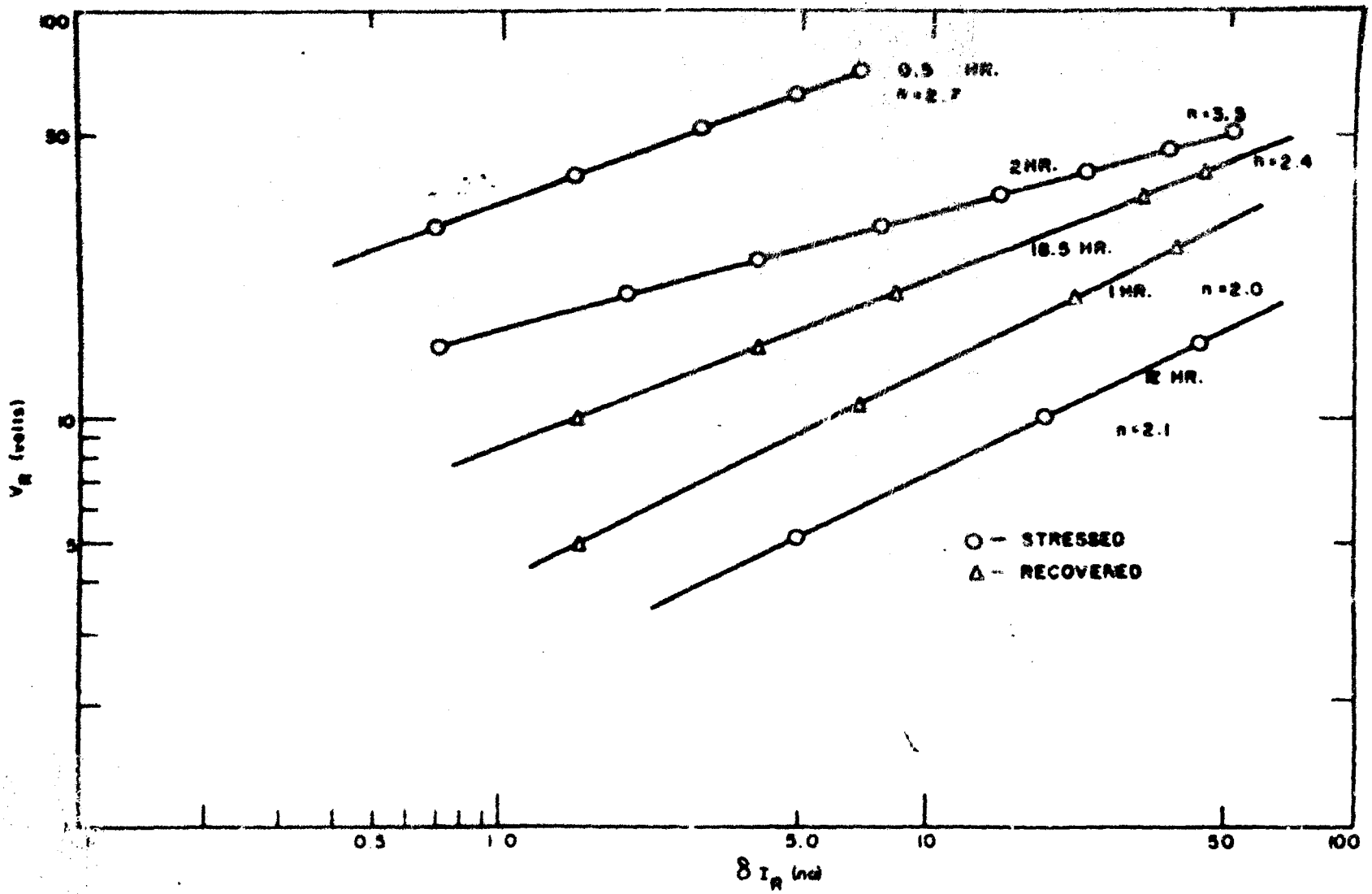


FIGURE 4

LOG-LOG PLOT OF POWER LAW DEGRADATION

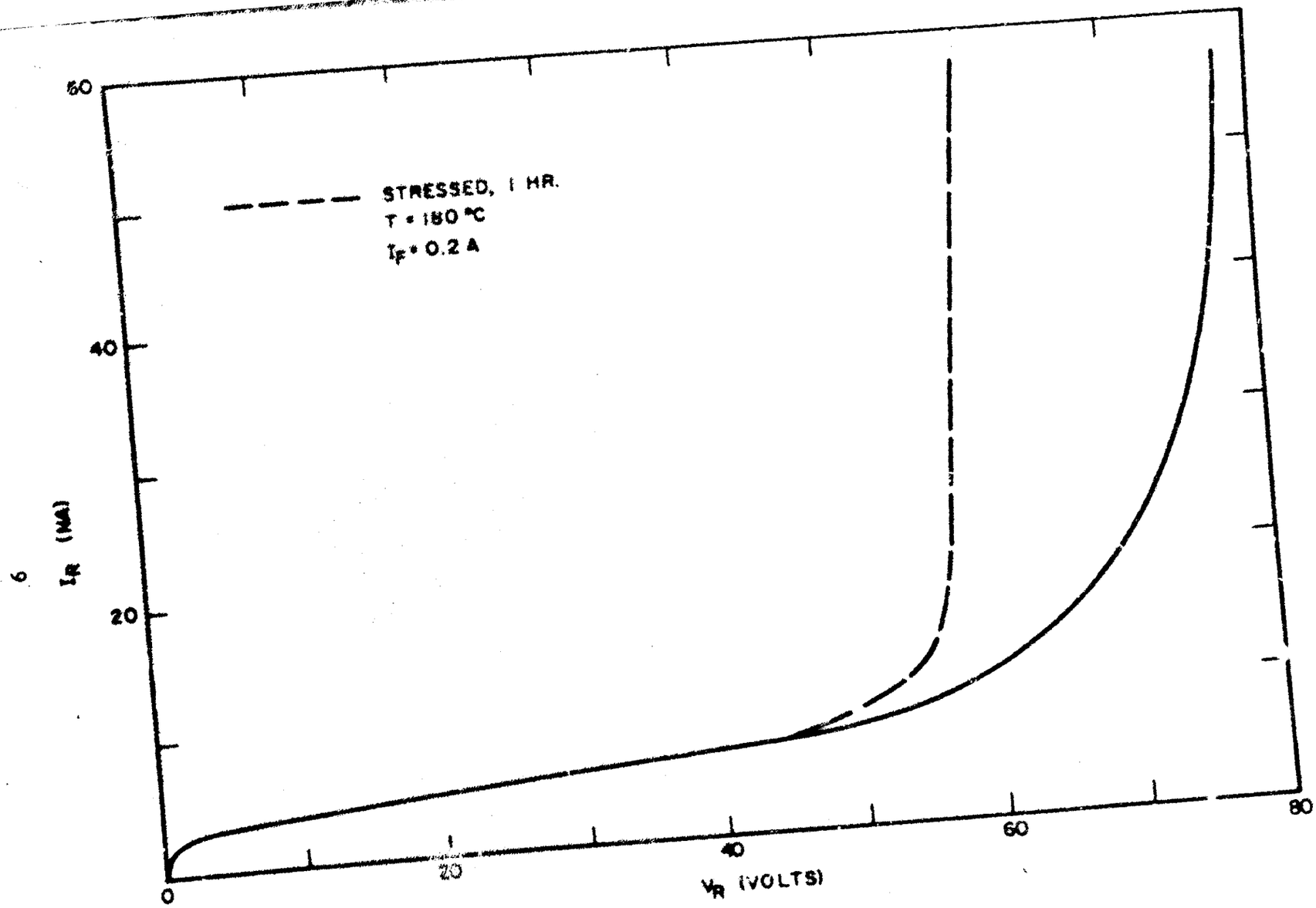


FIGURE 5

ABRUPT ONSET OF EXCESS REVERSE CURRENT

increased rapidly. Observation of the excess current at higher levels than those shown in Figure 5 demonstrated that the excess current was approximately linear with voltage and that no decrease in the high current (above 1 milliampere) breakdown voltage had occurred. It was found that continued stressing could result in a decrease in the critical voltage, but often the result of continued stressing was the gradual appearance of a power law degradation at low voltages. Heat treatment at 440°C without bias usually resulted in an increase in the critical voltage, but not in the complete recovery of the diode.

A third behavior found in ten to twenty per cent of the diodes was the absence of any detectable degradation in reverse current below eighty volts, even after prolonged forward current stress.

The same modes of degradation could be observed at lower ambient temperatures, although longer duration stresses were required. With a room temperature ambient, it was found that a forward current of 300 milliamperes would produce significant degradation in most units in less than a day and very severe degradation within a week. The failure modes discussed above were the only ones detected for forward currents up to 300 milliamperes and temperatures up to 210°C. The rate of degradation was, of course, dependent on temperature and current. At room temperature the same failure mode applied to even higher current levels. Figure 6 shows the rapid onset of degradation at a current level of 500 milliamperes, at room temperature. It is seen that the diode could withstand this current for periods of less than a minute, but severe degradation resulted from the longer stresses. The degradation would have been even more rapid except that the diode was walked out after each period of stress

(the phenomenon of walkout is discussed in detail in paragraph 1.4). As the current was increased, similar degradation was experienced but it occurred more rapidly, with 30 seconds at 0.9 amperes forward current being roughly equivalent to 35 minutes at 0.5 amperes. Thirty seconds at 1.2 amperes produced a new type of failure, but rectification was still present and the diode drew 3.5 microamperes at a reverse voltage of 30 volts and 180 microamperes at a reverse voltage of 60 volts. Thirty seconds at 1.5 amperes resulted in a shorted junction, with a resistance of 0.05 ohms, which was the series resistance expected from the epitaxial material beneath the junction. The junction temperature at the 1.5 ampere current level probably resulted in the alloying of the silver contact and the silicon which then resulted in the shorted junction. It is important to note for the situation shown in Figure 6 that when the characteristic was measured at high current levels (in the vicinity of one milliampere) it was found that the junction breakdown voltage was unchanged from the prestress value.

To investigate the room temperature response to forward bias stressing, four diodes were subjected to a forward bias of 300 milliamperes at room temperature ambient along with two double heat sink diodes manufactured by a vendor other than General Electric. One of the General Electric diodes remained stable under this stress for over a week and gave no indication of failure. The other three diodes degraded badly after 20 to 40 hours of this stress. The diodes manufactured by the other vendor also failed, with a rate and magnitude of degradation very similar to the three General Electric diodes. The mode of failure appeared to be identical to the degradation of diodes under forward bias at high

temperature. In the first few hours, the diode characteristic hardened slightly prior to the onset of degradation.

There is an important comparison between characteristics of the unstressed diodes in Figure 2 and those of the degraded units in Figures 3,4 and 6. It is seen that unit I in Figure 2 had a characteristic which resembled that of an initially harder diode which had undergone a substantial amount of power law degradation. Unit II had a characteristic which resembled those of degraded units which had a rapid current increase above a critical voltage. This was confirmation of the idea that the degradation which accompanied the sealing process, and which necessitated the annealing and aging process, was of the same nature as that observed following forward bias degradation. It also indicated that the annealing and aging process did not completely remove this degradation. This comparison also required that any attempt to calculate the reverse voltage-current characteristics of the unstressed diodes must allow for the presence of an excess current component. This component could not be attributed to uniform or nearly uniform pre-avalanche multiplication in the high field region between the junction and the sub-epitaxial layer, since the breakdown voltage of this region was known to be unaffected by stress.

The temperature dependence of the excess current is shown in Figure 7. The solid line shows the behavior of the generation current in the undegraded diode. The high temperature slope corresponded to an activation energy of 0.71 ev which was which within the experimental error of earlier observations for silicon P-N junctions.[1] The change of slope below room temperature was due to the freezing out of free carriers onto the dopant ions. It is seen that the excess current resulting from forward bias

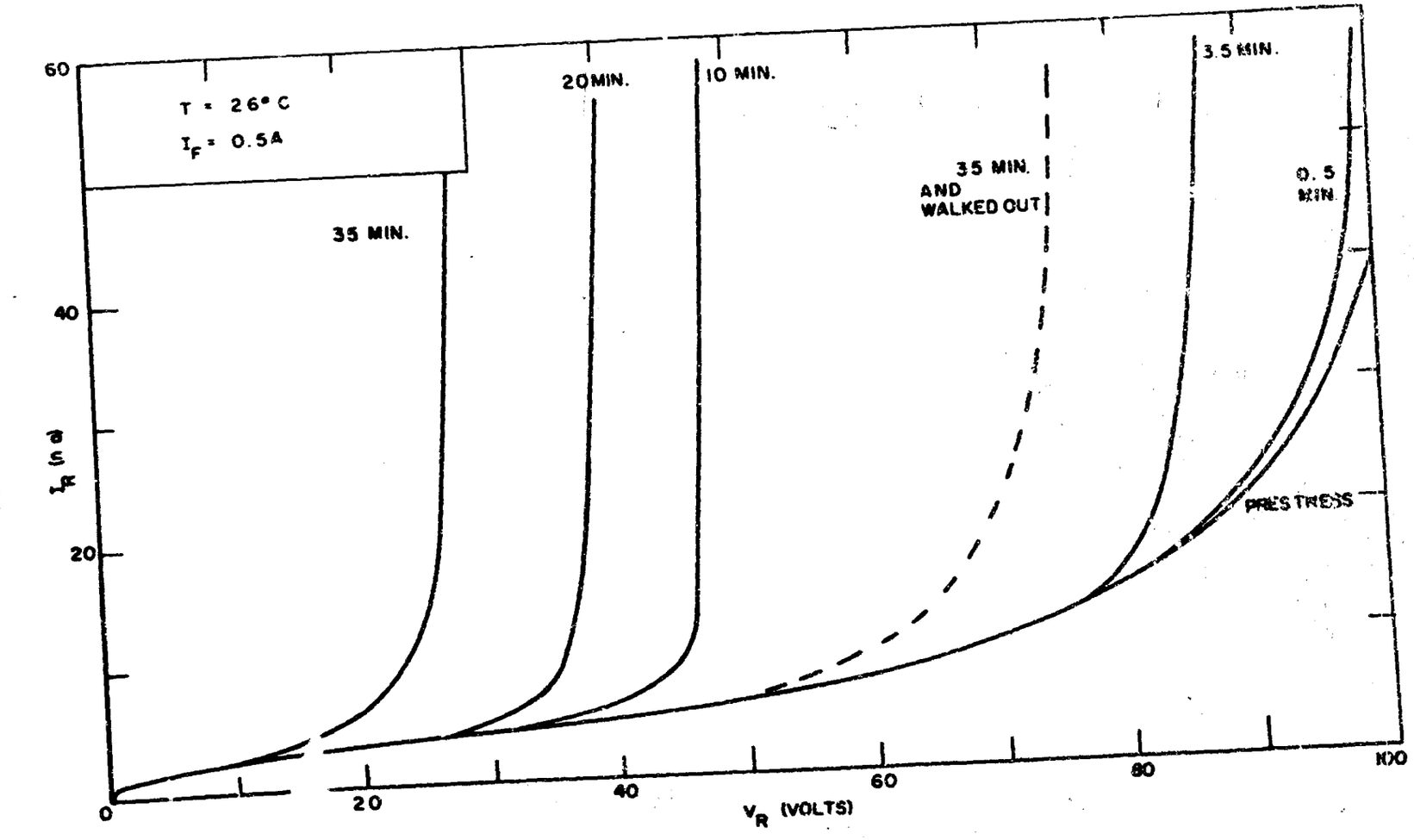


FIGURE 6

RESPONSE TO VERY HIGH FORWARD CURRENT

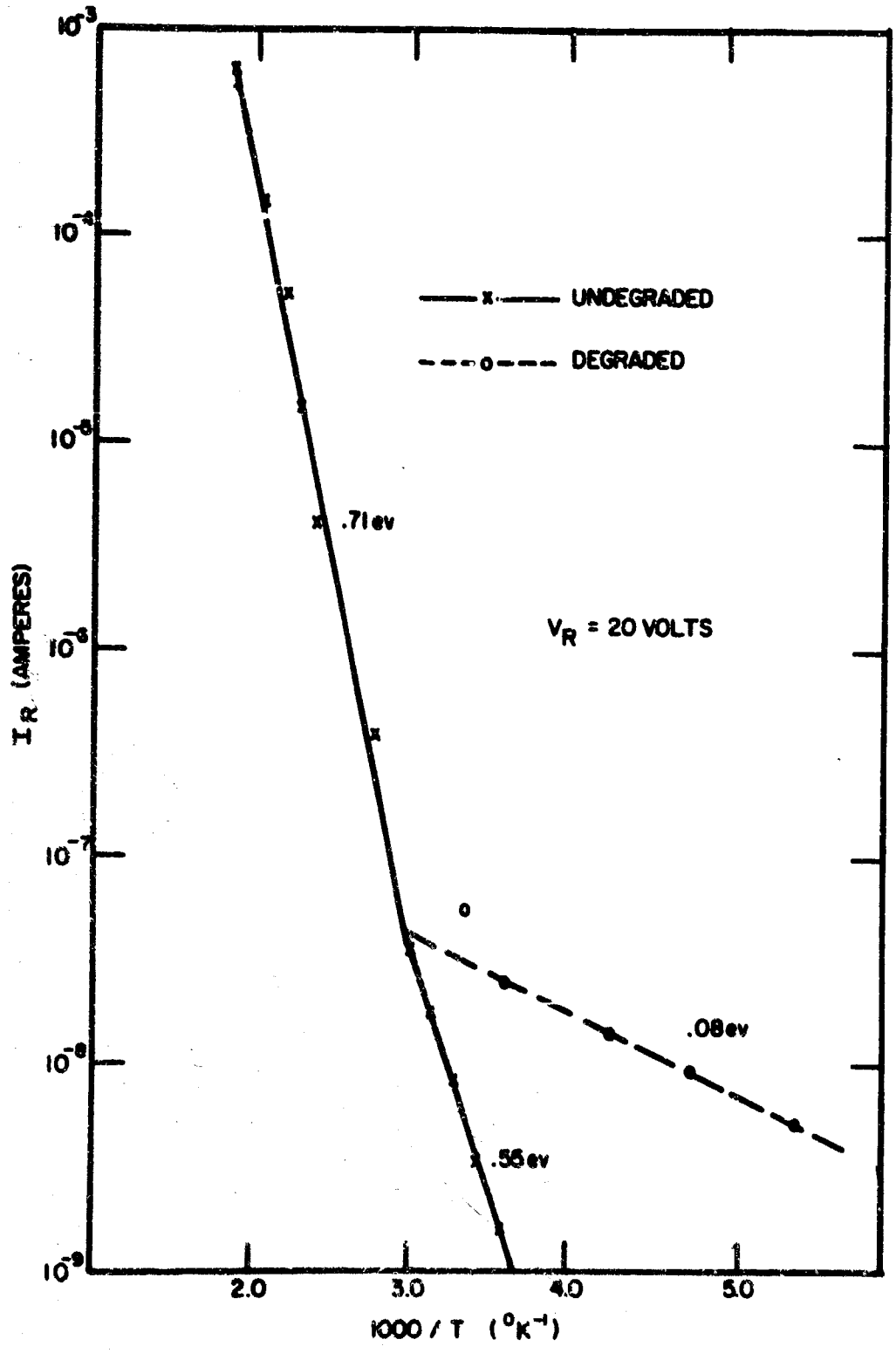


FIGURE 7

ARRHENIUS PLOT OF REVERSE CURRENT FOR DEGRADED AND UNDEGRADED DIODES

degradation was less strongly temperature dependent than the junction generation current. This was different from the excess current following reverse bias degradation, which showed the same temperature dependence as the generation current. The activation energy of .08 ev was not a constant, but was smaller for higher measuring voltages, where more excess current flowed. The weaker dependence on temperature made the observation of excess current caused by forward bias degradation at elevated temperatures more difficult than in the reverse bias case, because at high temperatures the component due to forward bias degradation was small compared to the junction generation current. However, in heavily degraded diodes, excess current caused by forward bias degradation could be observed at 140°C. Unlike the case of the reverse bias failure mode, this technique has not proved useful for determining rates of degradation.

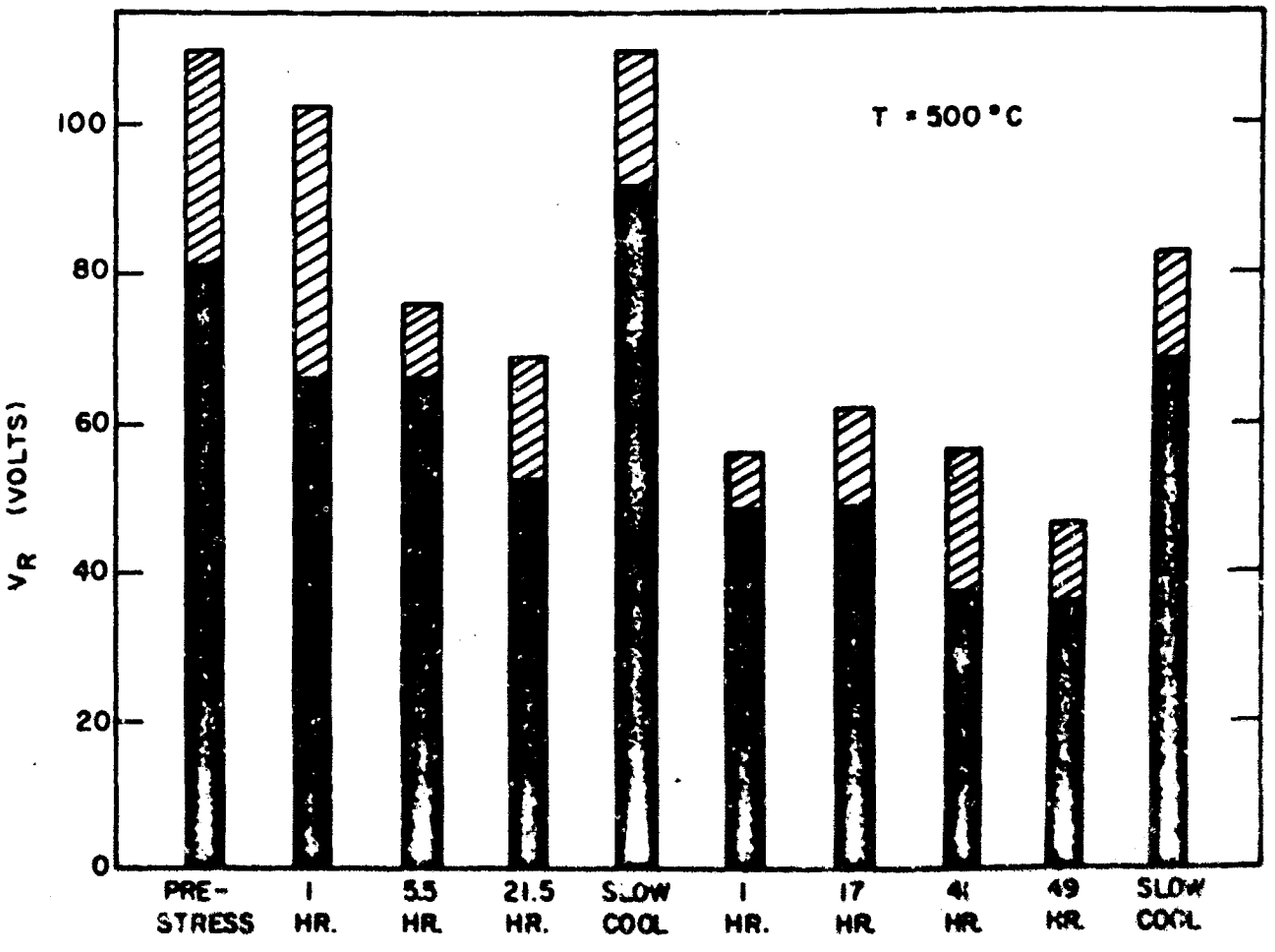
1.3 High Temperature, Zero Bias Stresses

It was found that heating the diodes into the range of 400°C to 550°C, with no applied bias, resulted in a degradation of the room temperature reverse current characteristic which was identical with that produced by forward current stressing. Both power law and abrupt increases in the reverse leakage current were observed but units showing power law degradation were less common. It was found that the extent of the damage produced by zero bias heating was completely different when the diode was cooled slowly from the elevated temperature (over a period of five hours) than when the diode was cooled rapidly, or quenched, (in a period of 5 to 10 seconds) by placing it on a large room temperature heat sink. In the former case, not much degradation, and often an improvement, was observed. However, when the diode was quenched from the high temperature, degradation was always observed.

Figure 8 shows the behavior of one diode which was subjected to repeated periods at 500°C. The cross hatched bars show the reverse voltage which was necessary to maintain a reverse current of 10 microamperes. The solid bars show the reverse voltage which was necessary to maintain a reverse current of 40 nanoamperes. The recovery which occurred when the diode was heated and slowly cooled is very evident. After the first slow cooling, it is seen that the reverse characteristic was even harder than it was before the temperature stress. The diode was quenched after each period at the elevated temperature except for the two cases marked slow cool. It may be seen that the major degradation took place in the first hour followed by a gradual degradation. This pattern was expected since other experiments had shown that most of the degradation at 500°C occurred in the first two minutes. After the diode had been heated and cooled slowly, considerable recovery was observed. This response pattern should provide information on the true temperature dependence of the mechanism responsible for the forward bias degradation.

The basic similarity between the forward current - induced degradation and the degradation caused by zero bias, high temperature stressing was established by the presence in both cases of walkout, microplasma noise, light emission and by the similar dependence of this excess current on reverse bias. During the second set of quenches shown in Figure 8, between 41 and 49 hours, the ambient stress temperature was raised to 550°C without markedly increasing the degradation.

In addition to degrading the room temperature reverse-current characteristic, the high temperature stresses affected the silver to silicon anode contact. In one case, after quenching the diode was open circuited



CROSS HATCHED BARS SHOW THE V_R NECESSARY TO MAINTAIN I_R AT 10μA. SOLID BARS SHOW THE V_R NECESSARY TO MAINTAIN I_R AT 40nA.

FIGURE 8

HIGH TEMPERATURE, ZERO BIAS STRESS AND RECOVERY

but contact was restored by another heating-cooling cycle. There also was a decrease in the low voltage current flow, indicating an increased contact potential. Heating the diodes to still higher temperatures (600°C) led to the flow of the sealing glass and usually to a change of position of the heat sink slugs relative to the silicon pellet. These distorted diodes were usually open, or had large forward voltage drops, and for this reason 550°C was about the practical limit for heat stressing or annealing the diode. It should be noted that lead oxidation, while severe, was not a limiting factor in these heating experiments because of the short stress times.

1.4 Walkout

A recurring feature of the forward bias failure mode was the presence of walkout (or push) which was a spontaneous hardening of the reverse voltage -current characteristic when large currents were first applied to the degraded diode. A typical walkout effect is shown in Figure 6. In the prestress condition, the reverse characteristic was stable and could be measured to currents above one milliampere without causing any instability. After a period of forward bias stress, an excess current appeared above a critical voltage which decreased with increasing stresses. It was found, however, that the excess current was not stable and if the voltage was held fixed just above the critical value, the current decreased rapidly toward the prestress value. Most of the decrease occurred in the first 20 seconds after the overvoltage was applied but a gradual decrease continued for about two minutes. If the measuring voltage was increased a volt or two, the whole process was repeated with the original measuring voltage acting as the critical voltage. This process could be repeated many times,

restoring nearly the prestress characteristic over a range of 30 to 40 volts. Walkout was accomplished more rapidly by applying a large overvoltage, sufficient to produce reverse current in the range from 100 microamperes to 1 milliampere. When this was done for one minute or so a large recovery in the low current characteristic was observed as shown on the dashed curve in Figure 6. After this period of walkout the reverse voltage-current characteristic was found to be stable up to the voltage at which the walkout was performed.

It was possible to record the progress of walkout as a function of time by connecting the diode to a constant voltage source and measuring the decreasing current or by using a constant current supply and measuring the increasing voltage. Figure 9 shows a semi-log plot of the results of the first procedure for a non-gold doped diode which had been stressed with a current of 200 milliamperes at a temperature of 215°C for 2 hours. The behavior was quantitatively like that observed in the gold doped diodes. A reverse voltage of 32 volts was applied when the critical voltage for excess currents was 28 volts. Instantaneously, a current of 1.7 microamperes floved which decayed in 5 seconds to 0.8 microamperes and in 10 seconds to 0.32 microamperes. From this point on, the time dependence of the current could be represented by:

$I_R = C_1 \exp(t/t_1) + C_2 \exp(t/t_2)$ where

$C_1 =$ 490 nanoamperes and $C_2 =$ 65 nanoamperes.

The time constants t_1 and t_2 were 17 seconds and 97 seconds respectively. Figure 10 shows the results of the procedure of maintaining a constant current of 2 microamperes while the voltage increased. Here, again, the walkout showed an exponential behavior with two components, one of which saturated more quickly than the other. The curve was accurately represented by :

$V_R = 75 - 23 \exp(t/270) - 19 \exp(t/15)$

where V_R is in volts and t is in seconds.

The walkout was observed in diodes after sealing and before the annealing and aging, in diodes which had been degraded with forward bias, and diodes which had been degraded with zero bias, high temperature storage. This was evidence for the common origin of all three types of degradation. In all three situations, the time dependence of walkout was similar and could be accellerated by increasing the overvoltage. Walkout was observed in diodes showing power law degradation as well as those with abrupt increases in reverse current. If walkout originated from localized heating, the excess current must have been very concentrated as walkout was often observed for currents less than 40 nanoamperes at voltages less than 40 volts where the total power into the junction was only 1.6 microwatts.

It is not clear, at the present time, whether the double exponential time dependence of the walkout represents a fundamental property or is merely a superficial effect. The time scale of the walkout is interesting because it requires a very long period compared to most electrical events in silicon and a very short period compared to ionic processes in silicon, or silicon oxide, at room temperature. It is possible that the walkout is related to the time dependent breakdown voltages observed in high voltage rectifiers.[2]

1.5 Microplasma Noise

The degradation resulting from forward bias stressing was suggestive of an avalanche breakdown mechanism and, for this reason, a search was made for the random, rectangular noise pulses known to accompany such breakdown. The

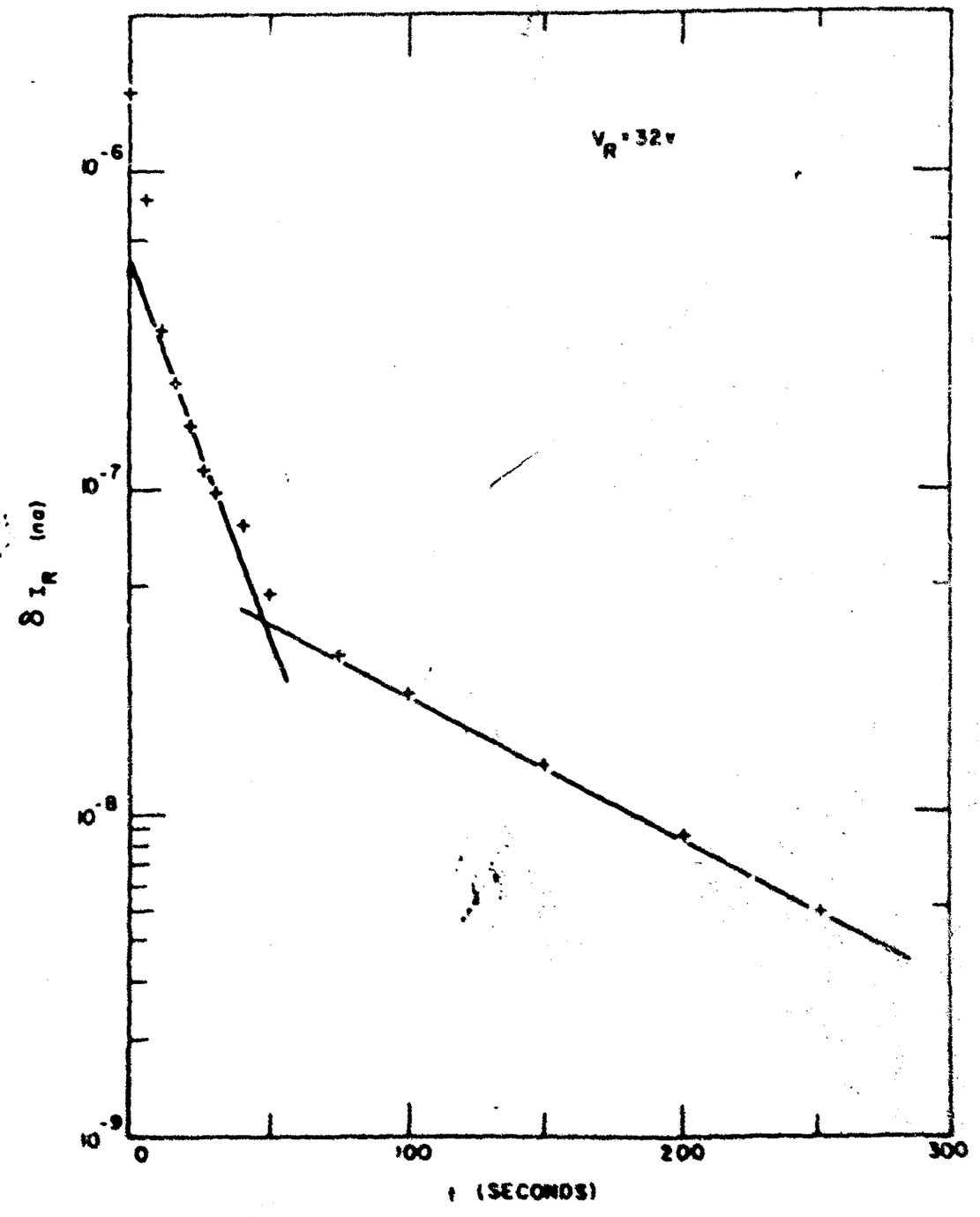


FIGURE 9

WALKOUT - DECREASING CURRENT AT CONSTANT VOLTAGE

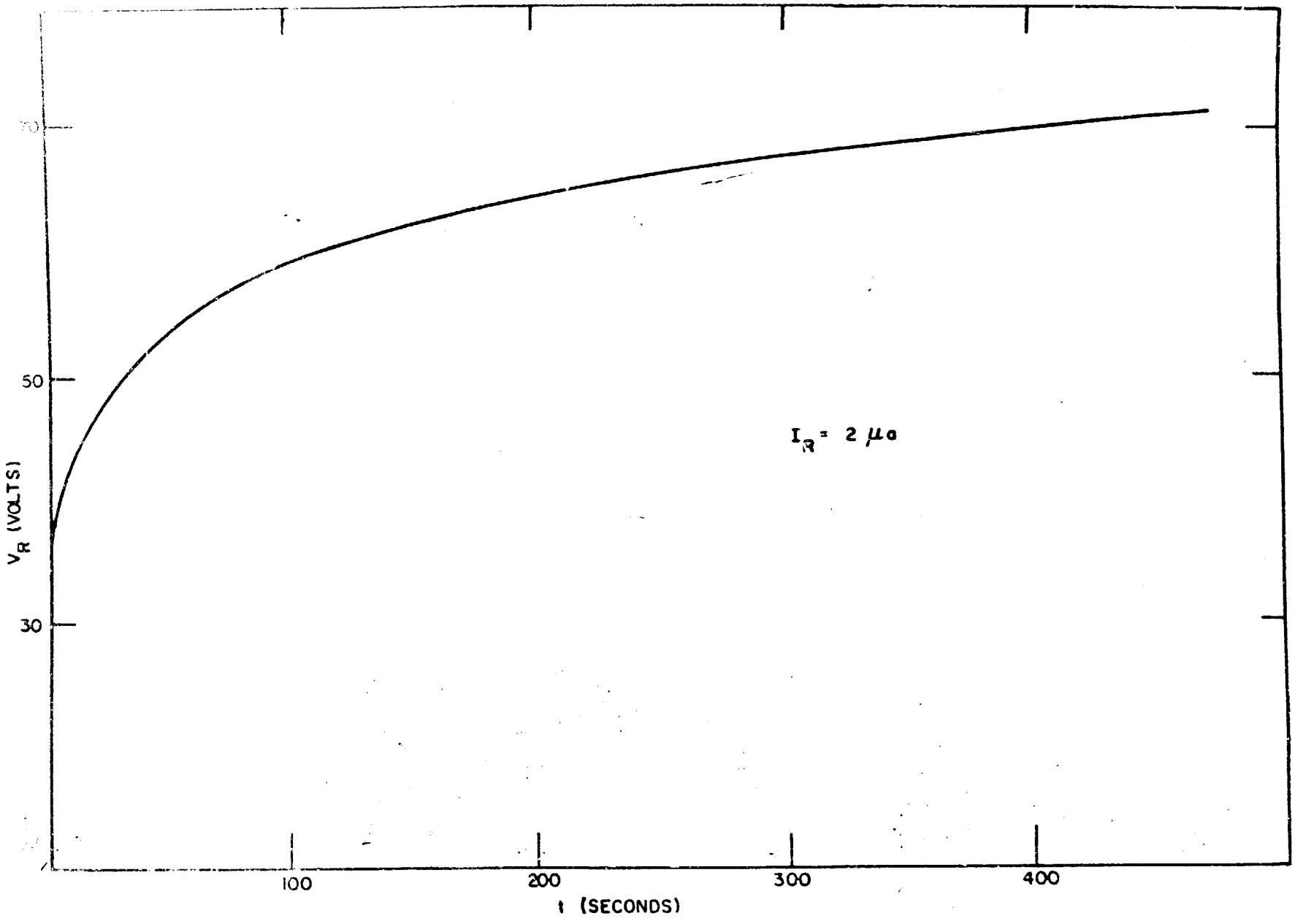


FIGURE 10

WALKOUT - INCREASING VOLTAGE AT CONSTANT CURRENT

reverse current of the degraded diodes was found to have a large noise component and, in about 10 per cent of the units studied rectangular current pulses were observed.

In gas discharge physics, the highly conducting regions of a neutral gas are referred to as a plasma and by analogy Rose[3] designated small, highly conductive, regions of P-N junctions as microplasmas. Microplasmas result from the presence of some defect near the junction which causes this local breakdown voltage to be smaller than the value characteristic of the junction as a whole. Consequently, as the reverse voltage is increased above a critical value the microplasma goes into avalanche and large reverse currents can flow, although the reverse voltage is less than the true junction breakdown voltage. The current resulting from a single microplasma is piece-wise linear, and is given by:

$$I = (V_R - V_0)\, R_S \qquad V_R > V_0$$

$$I = 0 \qquad V_R < V_0$$

Here V_0 is the breakdown, or turn-on, voltage of the microplasma and R_S is a series resistance which limits the current through the avalanching region. The current is, of course, superimposed on the normal reverse current of the rest of the junction. The resistance, R_S, is the sum of the spreading resistance of the path leading to the small breakdown region and a space charge component.[4] Microplasma breakdown is localized in regions one micron or less in diameter.

It is found that once a microplasma breakdown is initiated, it does not continue indefinitely even though the reverse voltage is held constant

at a value greater than V_0. Rather the current flows as a sequence of randomly spaced rectangular pulses [5,6,7]. The pulses are characterized by:

P_{01} - the turn on probability per unit time.

P_{10} - The turn off probability per unit time.

The reciprocal of P_{01} represents the mean time between pulses and $1/P_{10}$ is the mean pulse length. The two probabilities are voltage dependent with P_{01} increasing and P_{10} decreasing rapidly as the reverse voltage is increased above V_0. For overvoltages large enough so that P_{10} is very small, the pulse length becomes very long, the microplasma is turned on almost all the time, and the noise component of the microplasma current vanishes.

The circuit shown in Figure 11 was constructed to look for microplasma noise pulses. The resistor in series with the diode provided a voltage pulse across the oscilloscope input each time there was a current pulse generated in the diode. The circuit was built inside a metal box to reduce pickup noise and the signal was carried to the CRO with shielded cable. The shielding was not required for the smaller series resistors, but it was necessary when the 100 kilohm or 1 megohm resistors were used.

The diodes which had been degraded with forward current were found to contain an easily measured noise component in the reverse current. The maximum sensitivity of the oscilloscope used was 5 mv/division. Using this sensitivity, the noise was best observed across the one megohm resistor although it could be seen when the 10 kilohm resistors were used.

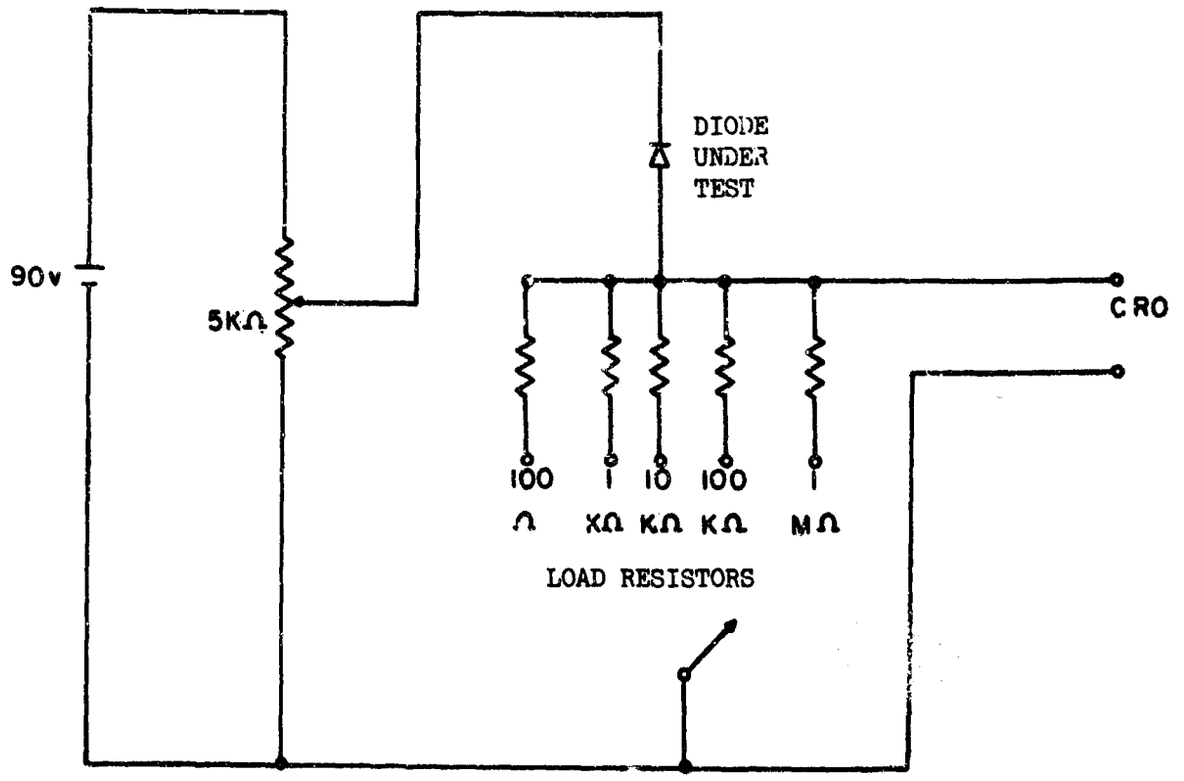


FIGURE 11

CIRCUIT FOR OBSERVING MICROPLASMA PULSE NOISE

The amplitude of the noise was voltage-dependent. There was no noise component for voltages below the onset of the excess current and the noise amplitude increased rapidly with voltage above this level. This noise was observed to accompany the excess current in the following types of unit:

1. diodes degraded by forward bias stressing (both in units showing power law and critical voltage types of excess current),
2. diodes degraded by zero-bias, high temperature stressing,
3. units which had been sealed but not annealed or aged,
4. units of the type I and II in Figure 2 which showed traces of damage remaining after annealing and aging.

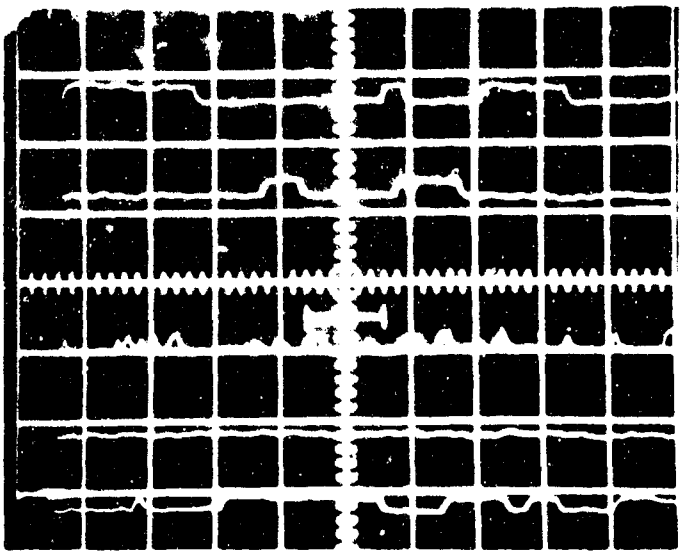
The noise being discussed should not be confused with the generation-recombination noise observed in all P-N junctions at all voltages, or with 1/f noise, as these noise types are of much smaller amplitude and require much more elaborate techniques for their observation.

Shown in Figure 12 are five separate traces of the voltage across the 1 megohm resistor as a particular diode was held at a constant reverse bias in the region of excess current. The vertical sensitivity was 5 mv/division and the horizontal sensitivity was 1.0 millisecond/division. If the traces are numbered 1 through 5 starting at the top of the photograph, it is seen that trace 1 showed three pulses, trace 2 showed two, trace 4 showed none, and trace 5 showed four, and the beginning of a fifth. The curvature of the leading and trailing edges was caused by the charging of various stray capacitances in the measuring circuit and it is seen that the time constant was about 0.1 millisecond. As the 1.0 megohm load resistor was in parallel with the oscilloscope, which also has a 1.0

megohm input impedence, the actual load resistor was 0.5 megohm. From the observed time constant, the series equivalent stray capacitance was 200 picofarads. Because of the large time constant, the measuring circuit would not respond faithfully to any pulse shorter than a few tenths of a millisecond. This is the reason for the non-rectangular pulses in trace 3, which shows a train of closely spaced short pulses. In all the traces, it is seen that there is a background component to the noise superimposed on the rectangular pulses. In many degraded diodes, the background component was much larger than that shown in the figure so that the presence of the rectangular pulses was obscured. The amplitude of the current pulse required to give a 1.5 millivolt pulse across a 0.5 megohm resistor was only 3.0 nanoamperes. The total current in the diode at this voltage was about 40 nanoamperes. This particular unit manifested power law excess current after the annealing and aging and did not require stress to initiate the noise behavior.

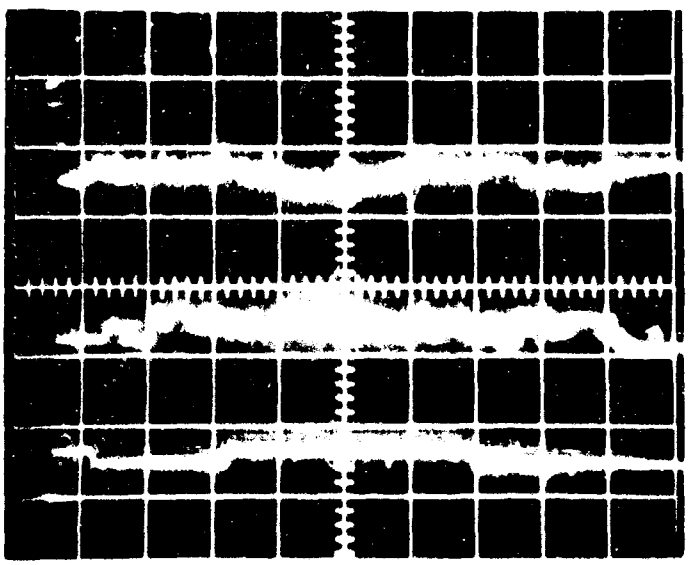
Figure 13 shows the response of a different diode, with a more common behavior, which exhibited several sets of superimposed pulses. The vertical scale was again 5 mv/division, and the load resistor was 1 megohm but the horizontal scale was 10 milliseconds/division. Except in the bottom trace, several sets of superimposed pulses are seen.

As the voltage across a diode producing rectangular pulses was increased, the rectangular pulses were replaced by a uniform background of large amplitude noise. This may be the result of the superposition of an enormous number of rectangular pulses. In most units only this background noise was observed, and no single set of pulses could be resolved.



MICROPLASMA NOISE PULSES

FIGURE 12



SUPERIMPOSED NOISE PULSES

FIGURE 13

The pulses observed in the degraded diodes and the microplasma pulses usually discussed in the literature had qualitative similarities and quantitative differences. The similarities between the two types of pulses were:

1. rectangular shape,
2. all pulses in a single pulse train were of the same amplitude,
3. pulses were of random length and there was a random interval between pulses.

The dissimilarities were in the magnitude of the current pulses, which are usually reported as being of the order of 50 to 100 microamperes in the literature, and were of the order of 10 nanoamperes in the degraded diodes. The series resistance is usually reported to be approximately 10 kilohms, while in the degraded diodes it was greater than one megohm. Conventional microplasmas produce pulses over a range of only one to four volts above the turn on voltage. In the degraded diodes, pulses, appearing to result from a single source, could be observed over a range of more than ten volts. The most important difference for reliability purposes was that, while most conventional microplasmas do not show a decrease in turn-on voltage when stressed, the stress-induced microplasmas in the degraded diodes showed a continual decrease in V_0 with increasing stress time.

For comparison, Figure 14 shows the voltage-current characteristic of a non-gold doped diode possessing a conventional microplasma. The vertical step in current near V_0 reflected the inability of the measuring equipment (electrometer and X-Y recorder) to follow the rapid fluctuation in the current just above V_0. This microplasma was not stress induced,

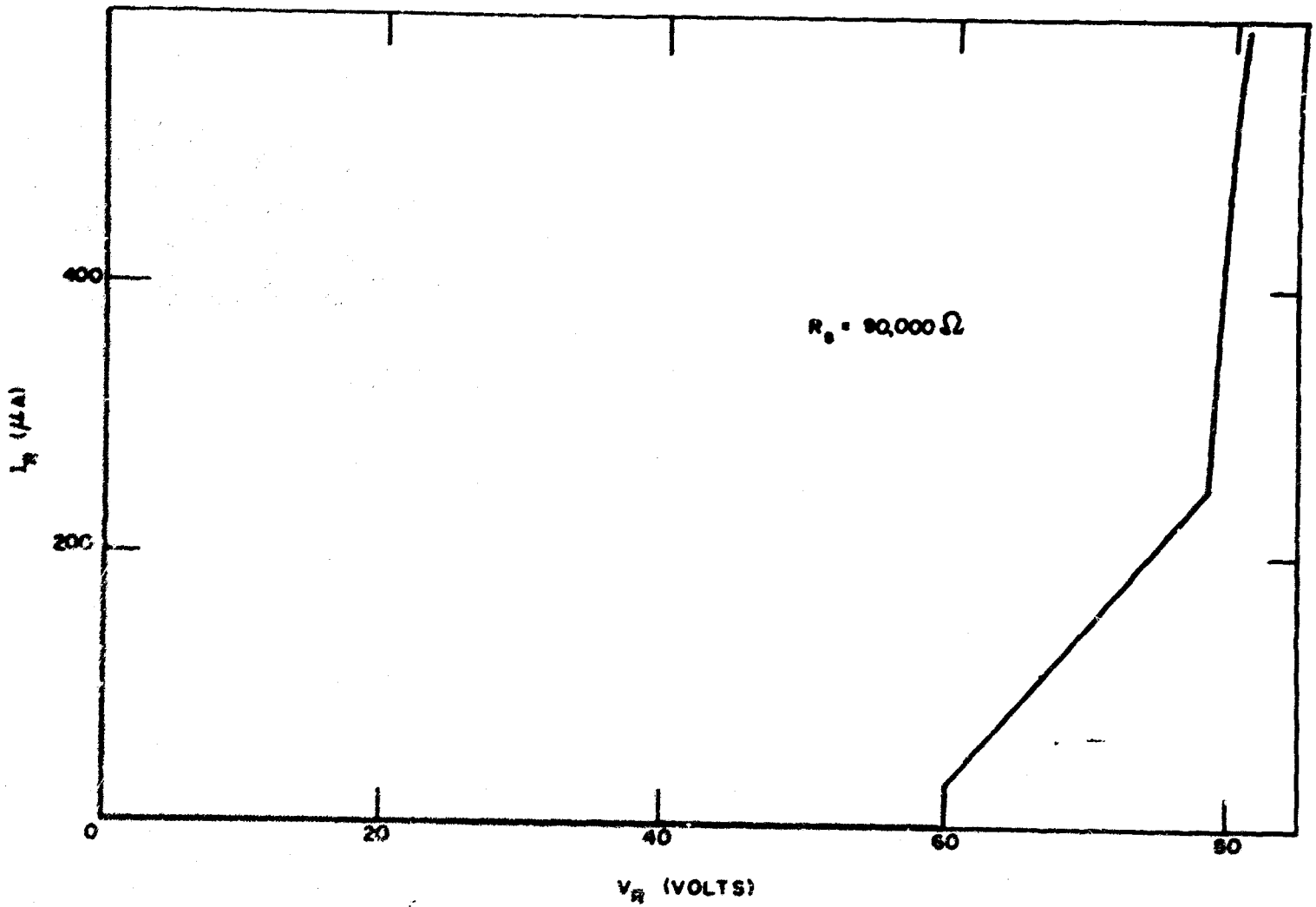


FIGURE 14

DIODE WITH CONVENTIONAL MICROPLASMA

but resulted from a manufacturing defect (diffusion spike or a gross surface defect). The diode showed pulses of a much higher amplitude (which could be observed across the 100 ohm resistor) than those of the stress induced microplasmas. The quantitative dissimilarities of the two types of microplasma may be due to differences in size of the region which is breaking down.

1.6 Light Emission Studies

The objective of these studies was to observe any light emitted during breakdown; determine the location of the light source; and to try to obtain a correlation between the light emission and the nature of the reverse characteristics of the diodes. Initial studies were carried out to determine the conditions under which light emission could be observed. The diode pellets were removed from the glass envelopes and the silver buttons were lifted. A micro-manipulator probe was used to establish contact with the window area of the pellet, and a constant power supply was used to reverse bias the pellet. By controlling the current, rather than the voltage, it was possible to operate well into breakdown without danger of the current running away and destroying the junction. The biased pellets were observed in a darkened room using a 60 power binocular microscope.

Light emission was first observed from a number of degraded diodes at reverse current levels of 4 or 5 milliamperes. In these units, the light emission continued for a few minutes, or a few hours at most, and gradually faded out. The optical arrangement used in these initial attempts was not suitable for obtaining photographic records of the emission and the mag-

nification was not high enough to permit observation of the light at lower current levels. Therefore, in subsequent work, the diode pellets were mounted on transistor headers and a one mil-gold wire was bonded to the P region to provide the electrical contact. This made it possible to use the metallurgical microscope to observe the emission at magnifications as great as 800 and to photographically record the results.

When the technique had been established for observing the light emission from the diode pellets, a systematic evaluation of a series of diodes was initiated. Twenty-three diodes with various histories were selected, all of them degraded. The reverse characteristics of these diodes were measured; the pellets removed from the glass envelope and the silver buttons removed; the reverse characteristics were measured again using the probe; the pellets were mounted on the transistor headers with a wire bonded to the P region; the reverse characteristics were measured once more. Of the twenty-three pellets, thirteen were damaged in handling so that ten were examined for light emission. Table I lists the diode number, diode type and the type of degradation:

TABLE I

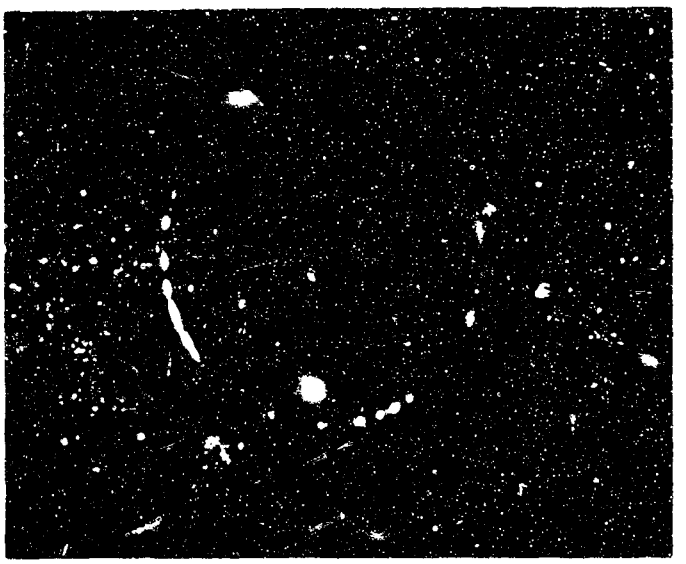
DEGRADED DIODES FOR EMISSION STUDIES

DIODE	DIODE TYPE	TYPE OF DEGRADATION STRESS
A-2, A-3, A-4	Gold Doped	500°C, 0 Bias
A-5, A-6, A-8, A-9	Gold Doped	Forward Bias
A-13, A-16	Gold Doped	Never Annealed
A-23	Non-Gold Doped	Forward Bias

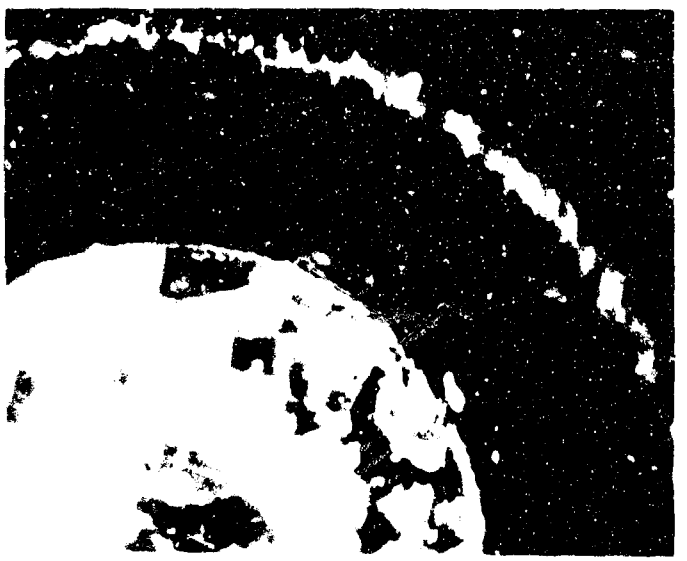
Light emission was observed from eight of the ten diodes. All five of the forward bias degraded diodes emitted light. For four of these five diodes, the light emission was observed as a continuous ring coindident with, or close to, the junction. The light emission from the other diodes appeared to come from discrete spots near the metallurgical junction.

The light emission from several of the diodes was photographed and Figure 15 is a photograph of the emission from diode A-3. The exposure time is unknown since the shutter was left open overnight and the emission ceased sometime during the night. The picture was taken with 4 milliamperes of reverse current through the diode and with approximately 200 X magnification. A well defined ring of discrete spots is visible.

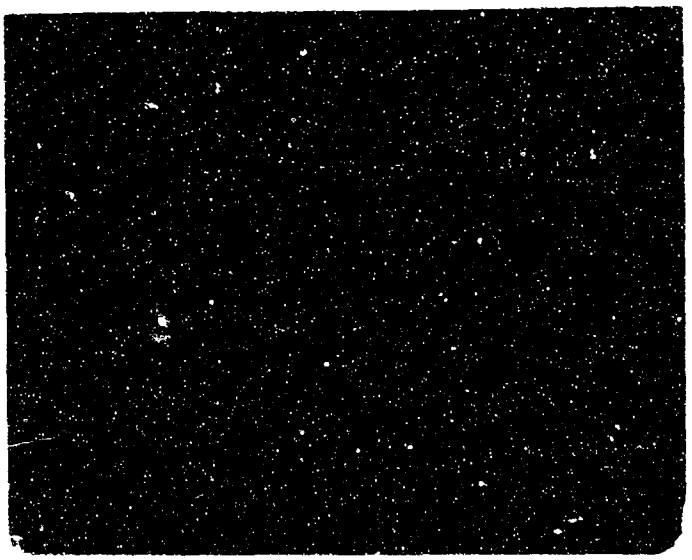
The light from diode A-8 was emitted in a continuous ring. This ring was bright enough so that it was possible to photograph it simultaneously with a dark field photograph of the pellet surface. The photograph is shown in Figure 16, which was a ten minute exposure with 2.5 milliamperes of reverse current through the diode and with an approximate magnification of 400 X. The edge of the window is clearly visible, as are the etch spots within the window. The irregular bright ring at the edge of the picture corresponds to the location of the edge of the silver button. The less bright ring concentric with the window edge is the light emitted by the diode. The distance of this ring from the window edge was measured using a reticle eyepiece on the microscope and found to be between 3 and 5 microns. This was close to the expected location of the junction at the diode surface. Figure 17 is a photograph of diode A-2 with a one hour exposure and with 1 milliampere of reverse current through the diode. The ring of discrete points of light is clearly visible.



DISCRETE LIGHT EMISSION
FROM DIODE A-3
FIGURE 15



CONTINUOUS LIGHT EMISSION
FROM DIODE A-8
FIGURE 16



DISCRETE LIGHT EMISSION
FROM DIODE A-2
FIGURE 17

An attempt was made to determine at what current level the light emission first became visible for three of the diodes. The lowest current at which any sample was found to emit was 10 to 15 microamperes (diode A-9). Diode A-2 emitted down to 35 microamperes, while A-5 emitted down to at least one milliampere. The emission gradually faded out and the currents were determined by the viewing conditions which prevailed during the experiment and must be considered only as upper limits. If these currents are converted to voltages, using the current-voltage characteristic curves for these diodes, it is determined that the lowest voltage at which emission was observed was 80 volts. All of the sources of light which were observed appeared to exist at or near the surface of the pellet, as indicated by several considerations. First, the light sources appeared to be in sharpest focus when the surface itself was in focus. The microscope is capable of discriminating to within about one micron in depth by adjusting the focus. Second, the light sources appeared to be white or yellow, whereas, if they had originated at any considerable depth within the silicon, selective absorption would have resulted in a red color. Finally the fact that the emission occurred very close to the expected intersection of the junction with the surface would also indicate that the emission is a near-surface phenomena.

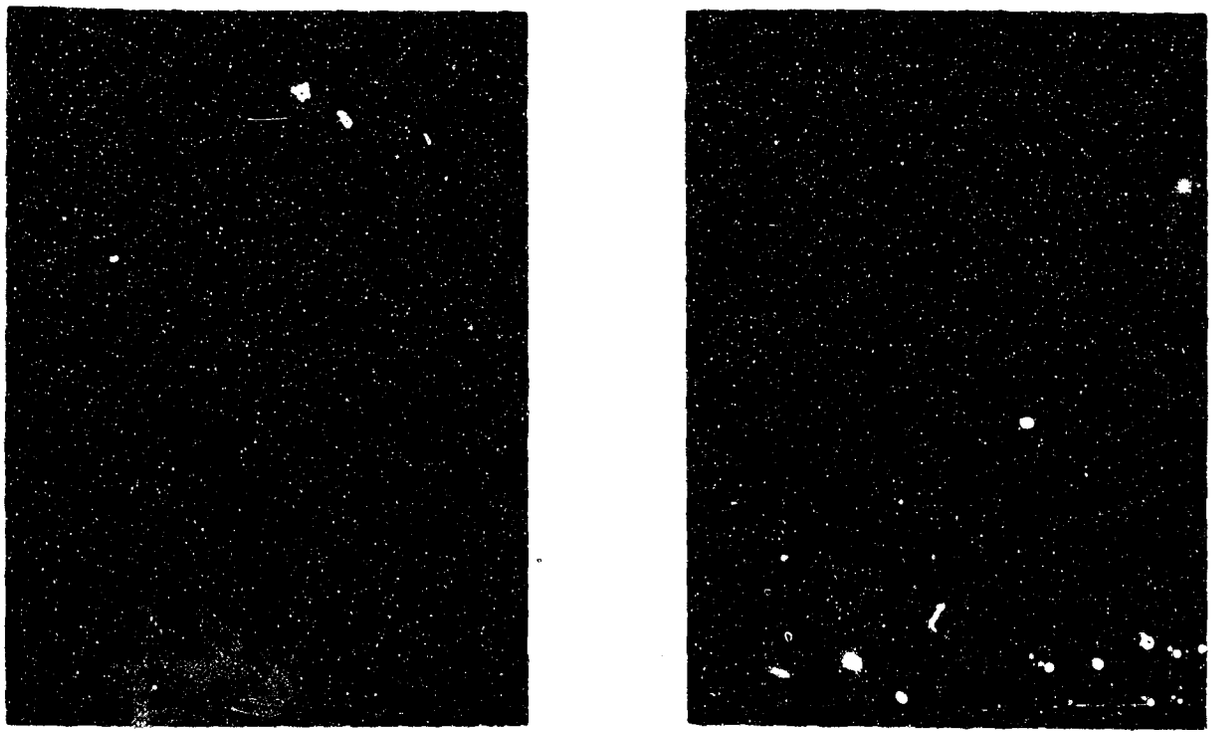
1.7 Etching Studies

The objectives of the etching studies were twofold. The first objective was to determine the effect of surface etching on the light emission from the diode; and second, to observe the effect on the reverse characteristics of degraded diodes as the oxide and silicon were progressively etched away. Four of the diodes which had previously been observed to emit light were

selected for the first etching experiment, A-3, A-8, A-9, and A-23. Each of these diodes were etched in HF for one minute to remove the oxide surface layer and then were examined under reverse bias for any changes in the light emission. Diode A-8 was observed to be emitting light, but the character of the emission changed from a continuous ring to a ring of discrete point sources of light. This is illustrated in Figure 18 which contains two photographs of the emission, before and after the etching. Both of these photographs were made with the same reverse current through the diode and with the same exposure. By reducing the current through the diode, while watching the emission through the microscope, it was possible to observe the emission at currents as low as 10 microamperes. The results obtained for A-9 were essentially the same as those for A-8. The A-23 diode appeared to be damaged by the etching, with cracks appearing in the silicon. The only emission seen after etching was one bright spot well into the window area. The A-3 diode lead wire was lost during the etching process and it was not possible to study the emission after etching.

The fact that the character of the emission was changed by etching of the oxide, for both A-8 and A-9 indicated that the emission was a surface phenomena. The fact that the emission during breakdown changed from a continuous to a discrete distribution will be useful evidence in formulating a physical model for the breakdown process.

In order to carry out the experiment in which the effect of etching on the reverse characteristic was observed, it was first necessary that a technique of etching and cleaning the silicon surface be developed. Contamination of the surface, especially with adsorbed moisture, can seriously



a) Before Etching of Oxide

b) After Etching of Oxide

EFFECT OF ETCHING ON
LIGHT EMISSION

FIGURE 18

degrade the diode reverse characteristic.

The first diode on which significant results were obtained was A-6. The reverse characteristic curves for this diode both before the degradation and after the surface etching are shown in Figure 19. This diode had not degraded appreciably under the forward bias. However, after etching the reverse characteristic was somewhat improved over the original, undegraded diode. The procedure followed in etching this diode involved a one minute etch in HF, followed by a two second etch in Iodine-B, and a quench in distilled water. The diode was then rinsed in flowing hot (200°F) distilled water for 10 minutes and soaked in acetone to remove the surface water. The diode was probed while still wet with acetone and the reverse characteristic was measured when the acetone dried. The surface was flushed with dry oxygen during the measurement to minimize the surface moisture.

Although this procedure was subsequently followed with several other diodes, in no case was it possible to reduce the reverse current below the degraded level, as had been observed with A-6. Four more diodes were degraded on forward bias, their reverse characteristics being measured before and after degradation. The pellets were removed from their envelopes and mounted on transistor headers. Two of the four pellets were damaged in the process. The two remaining diodes, B-2 and B-6, were etched following a procedure similar to that described above, but which included one additional step. After the etch in Iodine-B the diode surface was scrubbed with a detergent solution (alconox) before rinsing in hot distilled water. Instead of using acetone as the drying agent, ethyl alcohol was used. The results obtained are illustrated in Figure 20. The reverse characteristics for the degraded diode, B-2, are shown both before and after etching. As indicated, the

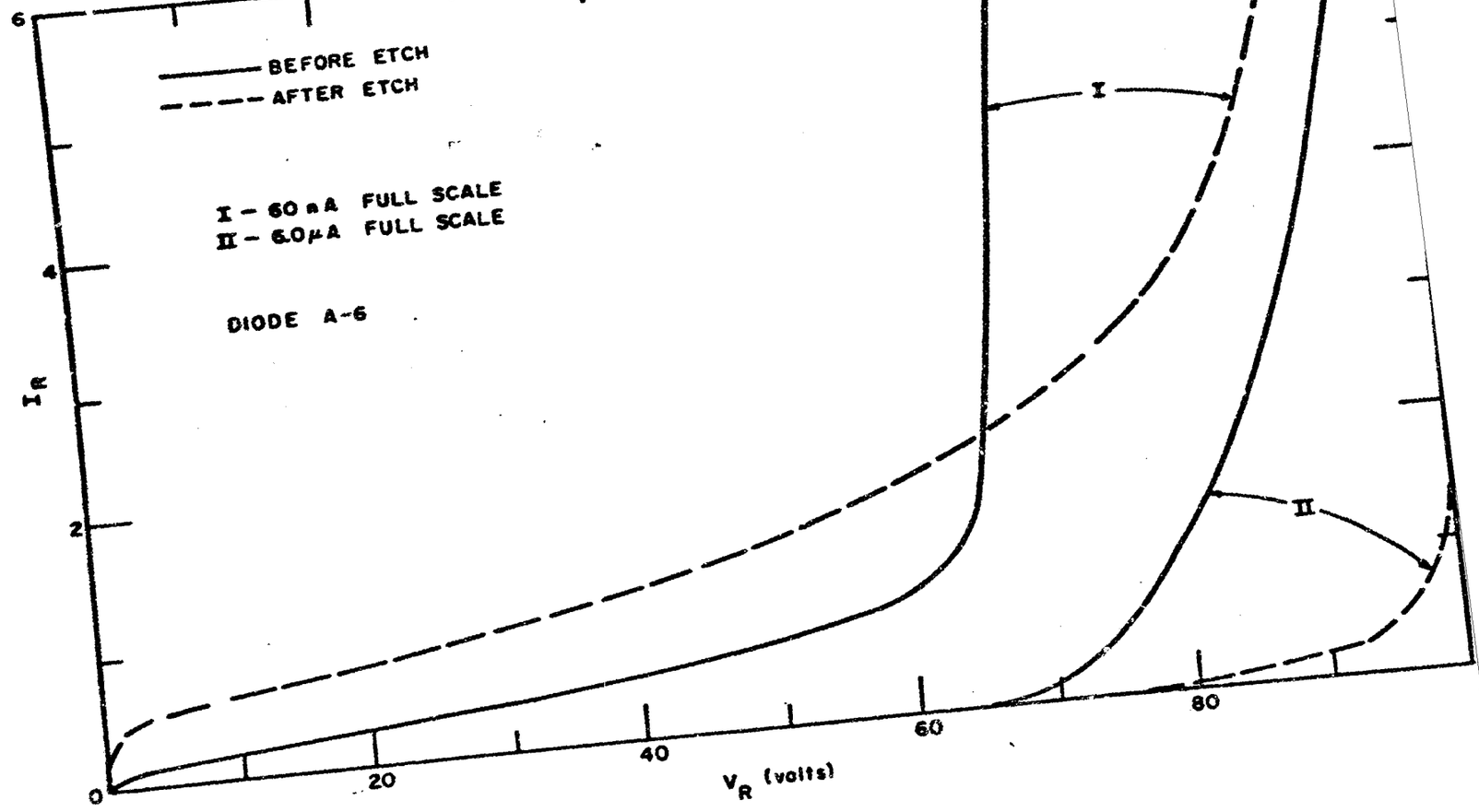


FIGURE 19

EFFECT OF ETCHING ON THE REVERSE CHARACTERISTIC OF DIODE A-6

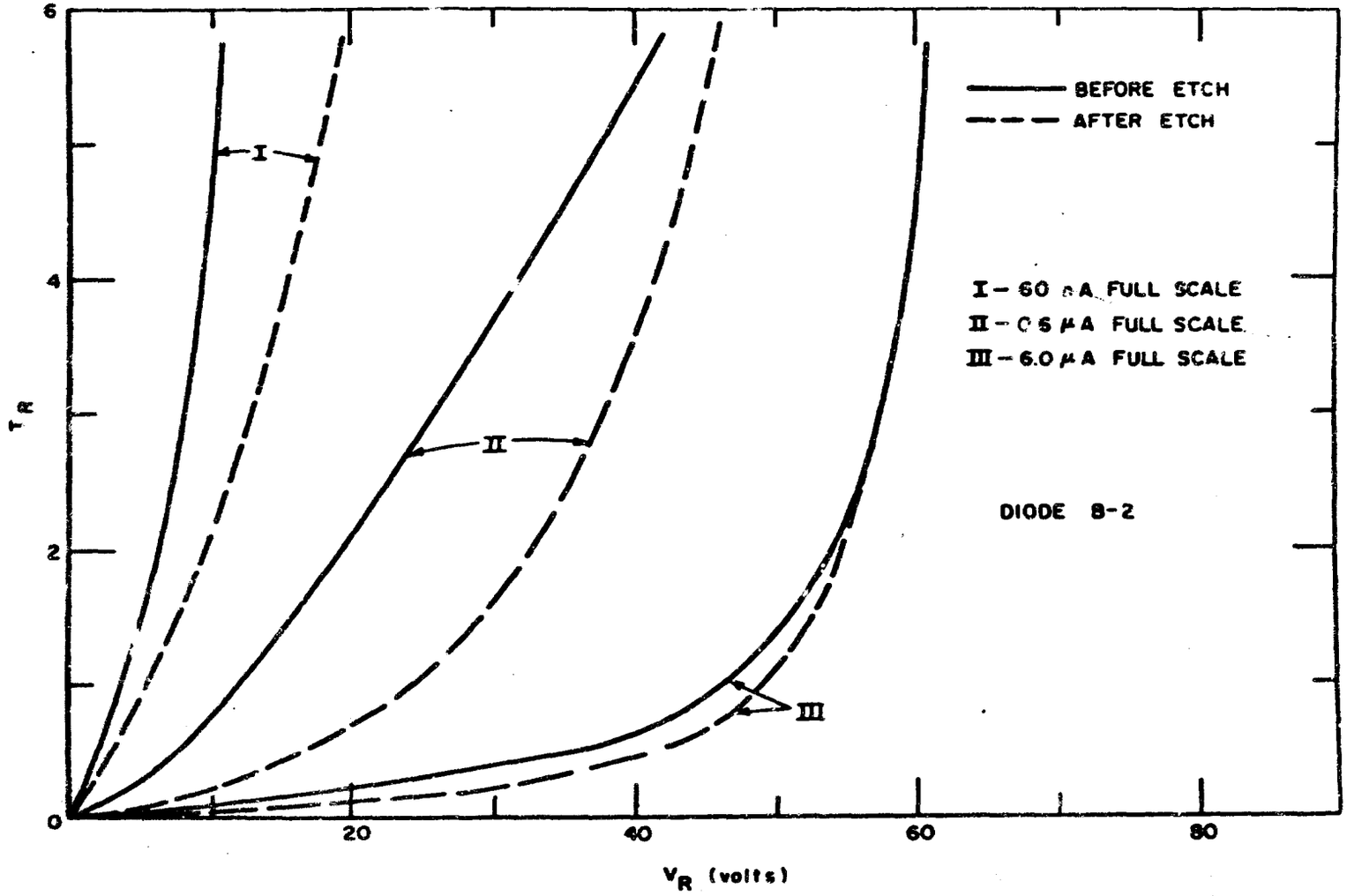


FIGURE 20

EFFECT OF ETCHING ON THE REVERSE

CHARACTERISTIC OF

DIODE B-2

etched diode was observed to have a significant decrease in reverse current compared to the unetched diode. However, only a part of the degradation was relieved by the surface etching. Whether this implies that only a part of the overall degradation is a surface effect is an open question. It is possible that part of the remaining reverse current was caused by surface contamination and could be eliminated when better cleaning procedures are developed.

At the present time it has been shown only that a part of the degradation is due to surface phenomena. Future effort will attempt to answer the question of whether or not the remaining degradation is also a surface effect. The approach will concentrate initially on attempts to determine whether forward bias degradation can be totally relieved by surface etching. This will involve attempts to assure that surface contamination is not contributing to the observed reverse current after etching.

1.8 Heat and Pressure Effects

Diodes which were constructed by mounting pellets on transistor headers did not degrade appreciably under normal forward bias conditions. These diodes were entirely similar to the standard diodes used in this study except that they had not been subjected to the heat and pressure encountered in the sealing process. Therefore, the temperature and/or pressure of sealing was suspected of producing changes in the pellet which led to failure when the diode was stressed with forward bias. A small testing jig was constructed to subject diode pellets to the sealing conditions and yet permit recovery of the pellet for mounting on a transistor header for further testing. The pellets were held between the polished ends of two

quartz rods. A movable heating coil was then placed around the rods, over the pellet, and heat and pressure could be applied as desired.

Several pellets were exposed to the normal sealing temperature and twice the normal sealing pressure and then mounted for test. Several other pellets were heated without pressure for comparison. Measurements of reverse characteristics were made on several pellets from each group immediately after treatment. Those which had been subjected to temperature only showed a slightly degraded characteristic at high reverse voltage, but this increase in current disappeared if the pellet was allowed to remain at room temperature for 30 minutes. The diodes which had both temperature and pressure exerted were quite erratic in their reaction to the stress. Some were highly degraded with walkout characteristics while others showed little or no degradation. Those with severe degradation were only slightly recoverable with a one hour heat treatment at 300°C.

After mounting on transistor headers, pellets from both groups were subjected to forward bias (0.2 amps at 180°C). The four diodes which had been heated only showed very little movement after four hours of this stress. One improved slightly, one degraded a little and two did not change. This behavior is typical of untreated pellets on transistor headers. The five diodes which had been exposed to both heat and pressure reacted quite differently. One remained constant while another degraded slightly. The other three showed sharp degradation of the reverse characteristic after four hours at 0.2 amperes and 180°C.

The forward voltage drop at 100 milliamperes was measured to see if

those devices which failed had a high power load during forward stress. Those pellets which had been heated showed no difference from untreated samples. The diodes which had seen both heat and pressure had a higher average forward resistance.

It was concluded from this test that the pressure used in preparing glass encapsulated diodes can cause damage which leads to failure when the diode is subjected to high temperature and forward current.

1.9 Screening Procedure

The fact that a fraction (approximately ten per cent) of the diodes degrade very slowly (if at all) under moderate forward bias stresses indicates that the development of a non-destructive screening process to find these units would be desirable. At first, inspection of the diode initial condition was considered as a possible screening procedure. However, the initial softness of the diode is not a consistent guide to behavior under forward bias stressing. That is, diodes I and II in Figure 2 will not necessarily degrade more rapidly under forward bias stress than diode III.

Because of the differing response rate to forward bias stress, it is possible to use a moderate stress to separate the slowly degrading from the rapidly degrading units. A preliminary test of the idea was made by stressing at a forward current of 200 milliamperes and an ambient temperature of 180°C for two hours. Following this, the diodes were further stressed at 150 milliamperes and 125° for a week. As expected, the diodes which degraded rapidly on the first test continued to do so at the lower level, while the units which were most resistant to the higher stress

continued to be at the lower stress. The result is that a fairly rapid high temperature test can be used to select diodes which will be most resistant to long term degradation under forward bias stress. The amount of degradation for most units under the high temperature stress is small enough that the test may be considered non-destructive. The forward bias deterministic model test plan will provide much more information to evaluate the screening process.

1.10 Summary

The degradation patterns which were present following the sealing process, forward current stress, and high temperature storage at zero bias were identical. These patterns included an excess reverse current with a characteristic dependence on measuring voltage, microplasma light emission, low amplitude microplasma noise pulses and walkout. This degradation was found, after stress, only in those pellets which had been exposed to the temperature and pressure of the sealing process.

Of the various failure mechanisms proposed in the previous semiannual report, the chemical degradation of the transition region between the silicon and the silicon oxide resulting in localized regions of low breakdown voltage was most likely to account for the present failure modes. With a measuring voltage, V_R, the total excess current caused by microplasmas was:

$$\delta I_R = \sum_i (V_R - V_i) / R_i$$

where V_i and R_i were the turn on voltage and the series resistance of the microplasma labelled i, and the sum included all microplasmas with V_i less

than V_R. In the cases of diodes showing no excess current below a well-defined critical voltage, all the V_i were larger than or equal to the critical voltage. This corresponded to the situation where light emission was confined to a single spot or a few spots. If there were a large number of breakdown regions, as in the cases when a continuous ring of light emission was observed, the sum in the expression for the δI_R could be approximated by an integral. If all the microplasma were taken to have the same series resistance

$$I = \int_0^{V_R} f(V) \frac{V_R - V}{R} dV$$

where f(V) is the distribution function for the microplasma breakdown voltages and f(V) dV is equal to the number of microplasmas breaking down between V and V + dV. If, for example, f(V) was taken to be a constant, independent of voltage, it was found that

$$I_R = f V_R^2 / 2R$$

This showed that a square law excess current could result from a superposition of many currents each of which was piecewise linear in voltage. If f (V) was not constant, but increased with increasing voltage, the excess current would increase more rapidly than the second power of the reverse voltage. In this model, power law approximations for the excess reverse currents were not fundamental, but were the result of a particular superposition of microplasma currents. For this reason, the distribution of exponents shown in Figure 4 would be the result of various distributions of microplasma breakdown voltages at each stage of stress and recovery.

Walkout can be explained as the gradual increase in turn on voltage with

time after a microplasma was turned on for the first time. Inspection of the reverse characteristics after walkout did not indicate a major increase in series resistance accompanying walkout. Thus, the primary stress dependent variable of an individual microplasma was the turn on voltage, which decreased with increased stress time. The walkout phenomenon was an increase in this voltage caused by the electric fields and local heating accompanying the initial breakdown of the microplasma.

The large excess currents resulting from forward bias stressing cannot be explained simply by an increase in the surface generation rate but require a more effective conduction mechanism. The most likely mechanism is the avalanche breakdown of small regions located where the junction intersects the silicon oxide layer. The effect of the sealing heat and pressure is to disrupt the transition region between the silicon and the silicon oxide. This includes the generation of dislocations in the silicon and, perhaps, small fissures near the interface. The resulting increase in the mobility of impurity species is believed to be a requirement for the device to be susceptible to forward bias degradation. It is for this reason that the pellets mounted on transistor headers which have not seen the sealing process are degraded much less rapidly than the fabricated diodes.

The chemical process occurring during stress to produce the microplasma regions is uncertain. Because of the presence of gold, phosphorus, boron, oxygen, and trace impurities such as sodium, in addition to silicon, the number of conceivable reactions is large. The possibilities are compounded by the presence of a disrupted lattice in the transition region. However, the occurrence of forward bias degradation in the non-gold doped diode

shows that gold is not required for the process. Recent work on the interaction of gold and phosphorus impurities in silicon [8] shows the potential, as failure mechanisms of solid state chemical reactions in silicon.

The high electric fields needed to produce avalanche breakdown at the silicon - silicon oxide interface require the width of the silicon space charge layer to be much narrower at the interface than in the bulk. At the interface the junction will be of the P+ N+ type rather than the P+N junction characteristic of the bulk. The electron concentration at the surface can be increased over that in the bulk either chemically, by the addition of donor atoms at the surface, or electrically, by the formation of positive ions in the silicon oxide.

The results of the high temperature, zero bias experiments indicate that a straightforward diffusion is not involved in the degradation as the degradation can be reversed by cooling the diode slowly rather than quenching it. This effect is compatible, however, with a model based on high temperature decomposition of a compound into components, at least one of which is active in increasing the surface electron concentration. Upon quenching, the components remain separated, but slow cooling results in their recombination and the recovery of the diode. Another possible, though less likely, explanation of the slow cooling experiments is a decrease of the residual stress in the pellet resulting from the annealing of the glass encapsulation.

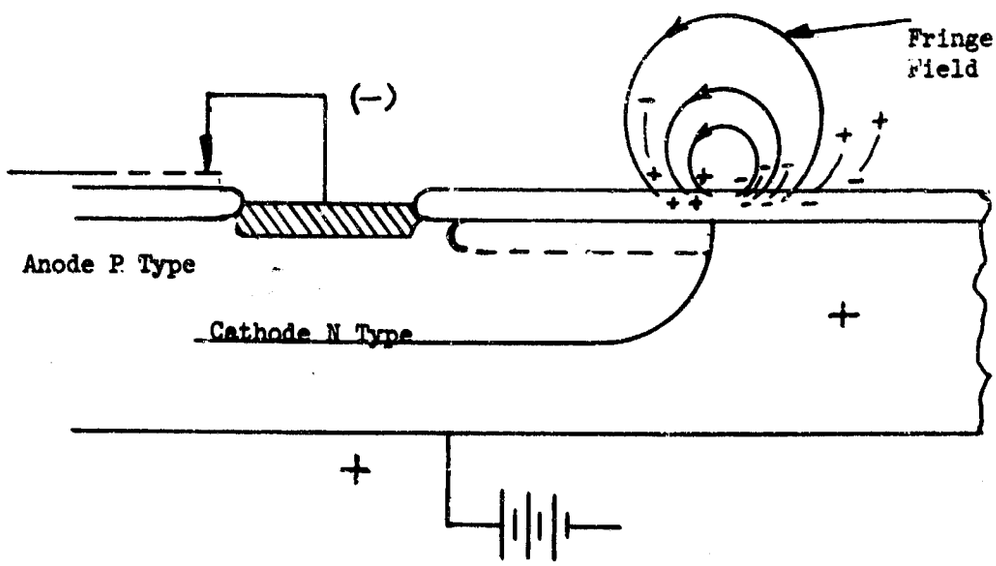
SECTION 2

FAILURE MECHANISMS AND ANALYSIS

2.1 Physical Nature of Failure Mechanisms

2.1.1 Type A-Surface Defects

Most failures of this type are attributed to inversion layers or accumulated surface charges on the junction. Reverse bias voltages, such as those applied in polarization tests, will set up surface fringe fields across the junction similar to those in a parallel plate capacitor. The fringe field can then line up dipole atoms or ions on dielectric silicon dioxide surface or within the passivation layer so that (-) charges face the cathode surface and (+) charges are aligned facing the anode.



As the sketch shows, the + charges lined up on the anode side of the surface will electrostatically attract electrons from the bulk. The accumulated charge may build up sufficiently at the surface to cause inversion of the "P" material to "N". A similar effect of opposite polarity can take place on the cathode surface. Note that when the inver-

sic. layer grows to meet the anode contact, a direct path from the anode to the cathode exists. Under reverse bias, this narrow surface channel effectively becomes thinner and eventually pinches off as the space charge region gets wider with voltage. This effect gives the reverse leakage characteristic a high saturating type of slope.

Since the mobility of the charges under the electric field will increase with temperature, the Type A failure mechanism is accelerated when voltage is applied under high temperature conditions. Units with Type A behavior can usually be completely recovered by heating without bias. The heat apparently serves to redistribute and disperse the aligned charges so that the unit recovers to the original characteristics.

If the oxide condition, or internal ambient, is such that the surface potential under thermal equilibrium conditions is extremely on the "N" side, a device may have low leakage before a high temperature test but will develop a Type A leakage characteristic as charges align to their equilibrium "N" condition under high temperature. In this case, both the surface potentials will have shifted toward "N". Thus, an "N" inversion and an N+ accumulation will lead to Type A leakage, together with a reduced or degraded breakdown voltage (now determined by the N+ resistivity). Measurement of the breakdown voltage after power tests, or other tests applying reverse bias to the junction, have maximum values determined by the bulk resistivity or junction defect spots. This occurs because the cathode tends to be pushed toward "P" or high resistivity "N" by the reverse bias.

2.1.2 Type B-Bulk Degradation

These units are usually characterized by a relatively high leakage at high

reverse voltages. At voltages of one volt or less, leakages may be low (0.5 nanoamperes or less) as compared to Type A rejects, which range upward from 10 nanoamperes at low voltages. It has also been found that these units are relatively unrecoverable by heating. Some improvement is often seen but this improvement is insignificant when compared with the 3 to 5 order of magnitude seen with Type A rejects. Since the breakdown voltages of these rejects is frequently degraded, it was at first believed that the rejects could be due to an "N" type condition induced on the cathode surface, which would in turn decrease breakdown voltage. However, the relative "stability" against recovery, together with an occasional tendency to degrade even further on breakdown voltage drive, leads to a speculation that the degradation is due to some change in the bulk; a crack or micro-alloy point through the junction. If a high leakage point exists in the junction, a high power test can result in point current density concentrations which finally lead to a runaway condition at the point in question. Dead shorts may be a severe form of Type "B" runaway.

Visual examination of Type B units frequently reveals the location of a bulk defect or failure. For example, visible "hot spots" under the alloyed contacts have been found, indicating where high current concentrations developed during the test period.

2.1.3. Type C and D - Bonding and Packaging Defects

The main mechanical failure mode for this design is an increase of the reverse leakage current due to partial shunting of the junction by the anode contact. When the device is fabricated, excessive pressure or poor

parts alignment during sealing may result in deformation of the glass and/or anode button such that the anode heatsink comes in contact with the edge of the pellet. Direct shunting of the diode does not necessarily occur at this time, as the passivation oxide electrically insulates the anode contact from the cathode pellet. Diodes with this internal "near shunt" have been found to fail when subjected to two different stresses. First, when subjected to mechanical or thermal shock, the anode may break through the insulating oxide layer and shunt the anode directly to the cathode. This results in a catastrophic increase in the reverse leakage. The second sensitive stress condition is a high temperature storage, such as 200°C. As the cathode is only separated from the anode by an oxide layer 10,000 angstroms thick, a small amount of moisture or mobile surface ions can easily bridge this short path and result in a slight, though not catastrophic, reverse leakage current increase.

2.1.4 Type E-Improper Measurement Procedures

Type E failures are frequently identifiable from visual evidence of unusual situations such as melted material. This class of failure generally results from an error in handling, an error in test equipment accuracy or calibration, or transients in the test equipment. An analysis of the circuitry involved generally reveals that the visually evident failure would have been impossible to obtain if the device had been properly connected to a circuit in good operating condition.

2.1.5. Type F-Thermal Overstress

Failures in this category have been traced to mild and severe overheating conditions beyond the physical limits of the materials used to fabricate

the device. These failures are found to be of two distinct types. One type is caused by a thermal fatigue condition where very slight alloying or diffusion of the materials occurs. This type is characterized by a mild increase in reverse leakage current. The other type of failure occurs due to a thermal runaway condition which causes gross alloying of the device materials and causes a dead short very similar to some of the E type failures. Both types of thermal overstress failures are generated on tests considerably above maximum operating conditions and do not represent an acceleration of an existing failure mechanism.

2.2 Failure Mode Chart

The next several pages contain a Failure Mode Chart which has been developed to define and illustrate failure mode categories, failure mechanisms and failure causes. The chart also shows the most likely failure indicator and the stress which generally causes the failure. The failure code shown in the charts is used in all the Failure Analysis Reports.

The Failure Mode Chart was developed to cover all the possible failures of the diodes and thus contains some failure codes which have not been observed in this program.

FAILURE MODE CHART

SILICON PLANAR DIODE.

Failure Mode Category	Failure Indicator & Stress	Failure Mode	Failure Mechanism	Failure Causes
A. Pellet surface degradation	2 to 50-fold increase in reverse verse leakage current and/or capacitance shift when stressed in reverse polarization and/or operating life tests, particularly at high temperature.	1. Inversion layers in silicon	a) "P" Inversion of N Surface	1) Defects in oxide passivation 2) Improper wafer cleaning 3) Contaminated diffusion boats 4) Improper cleaning of diffusion tubes and fixtures 5) Contaminated gas supplies 6) Contaminated diffusion sources 7) Improper pellet cleaning 8) Contaminants from diode parts
		2. Surface contamination	a) "N" Inversion of "P" diffused surface or N+ accumulation on N Surface.	1) Defects in oxide passivation 2) Improper wafer cleaning 3) Contaminated diffusion boats 4) Improper cleaning of diffusion tubes and fixtures 5) Contaminated gas supplies 6) Contaminated diffusion sources 7) Improper pellet cleaning 8) Contaminants from diode parts
			b) Mobile surface ions causing ionic condition	1) Contaminated gas supplies 2) Improper wafer cleaning 3) Improper pellet cleaning 4) Contaminated diffusion fixtures 5) Contaminants from diode parts

FAILURE MODE CHART — SILICON PLANAR DIODE

Failure Mode Category	Failure Indicator & Stress	Failure Mode	Failure Mechanism	Failure Causes
A. Pellet surface degradation Cont'd		3. Improper surface oxidation or passivation	a) Defects or Imperfections in SiO_2 layer and/or contaminants between Si-SiO_2 interface	1) Improper wafer cleaning 2) Contaminated oxidation fixtures 3) Defective KPR masks 4) Faulty oxide etching 5) Improper KPR removal
		4. Over alloy	a) Surface Inversion occurring in over alloyed areas	
B. Pellet Material degradation	Drastic upward shift in reverse leakage current and a change in forward voltage when stressed at high forward current bias, particularly at high temperature.	1. Defects in substrate or epitaxial silicon	a) Localized heating causing a hot spot and subsequent alloying or diffusion	1) Faulty cleaning of substrate material before epitaxial deposition 2) Flaw in crystal structure of substrate material
		2. Cracks or chips in critical area of pellet	a) Excessive strain on or in pellet	1) Improper scribing techniques 2) Oversized pellet 3) Undersized diode case 4) Flaw in pellet surface 5) Glass annealing step not performed properly 6) Flaw in pellet edge 7) Improper handling of pellets 8) Improper pellet loading 9) Improper application of assembly weights
		3. Irregular contact	a) Flaw in oxide window	1) Defective KPR mask 2) Improper cleaning in KPR process 3) Insufficient etching in contact process

FAILURE MODE CHART

SILICON PLANAR DIODE.

Failure Mode Category	Failure Indicator & Stress	Failure Mode	Failure Mechanism	Failure Causes
B. Pellet Material Degradation Cont'd		4. Defective Process over alloy	a) Localized heating in over alloyed spot causes bulk degradation	
C. Faulty Bond to Pellet	Large decrease in breakdown voltage and/or a large increase in reverse leakage current; slight increase in reverse leakage current and/or increase in forward current with characteristic indication of a low series resistance and when stressed in mechanical shock, vibration, thermal cycling, high & low temperature operation.	1. Faulty deposition of contacts	a) Pellet surfaces contaminated	1) Improper cleaning of wafers 2) Contaminated process solutions 3) Exhausted process solutions 4) Improper alloying techniques 5) Contaminated gas supply in alloy oven
			b) Insufficient alloying of contact to pellet	1) Insufficient etching before contact deposit
		2. Separation of contact from pellet	a) Pellet surfaces contaminated	1) Improper cleaning of wafers 2) Contaminated process solutions 3) Exhausted process solutions 4) Improper alloying techniques 5) Contaminated gas supply in alloy oven
			b) Insufficient alloying of contact to pellet	1) Insufficient etching before contact deposit
		3. Irregular Contact	a) Flaw in oxide window	1) Defective KPR mask 2) Improper cleaning in KPR process 3) Insufficient etching in contact process

FAILURE MODE CHART — SILICON PLANAR DIODE

Failure Mode Category	Failure Indicator & Stress	Failure Mode	Failure Mechanism	Failure Causes
D. Improper Packaging	Large decrease in breakdown voltage and/or a large increase in reverse leakage current; slight increase in reverse leakage current and/or increase in forward current with characteristic indication of a low series resistance and when stressed in mechanical shock, vibration, thermal cycling, high low temperature operation	1. Cracked or chipped pellet	a) Excessive stress on pellet	1) Improper pellet loading 2) Heavy weights used in assembly 3) Hold-down weight dropped in assembly 4) Oversize pellet 5) Improper scribing 6) Undersize glass case 7) Deformed anode contact
		2. Slugs misaligned	a) Leakage current path between anode slug and pellet cathode	1) Slugs not parallel with leads 2) Slug faces not flat 3) Slug faces not perpendicular to slug sides 4) Anode & cathode slug faces not parallel
		3. Improper slug contact	a) Low or deformed anode contract	1) Faulty contact process 2) Improper pellet loading 3) Heavy weights used in assembly 4) Hold-down weight dropped in assembly 5) Improper pellet cleaning 6) Improper parts handling
			b) Contaminants between slug & contact	
		4. Foreign materials inside package	a) Contaminants between slugs	1) Improper pellet cleaning 2) Improper parts handling
			b) Conduction path between anode contact or slug & pellet cathode	1) Improper pellet cleaning 2) Improper parts handling

FAILURE MODE CHART SILICON PLANAR DIODE.

FAILURE MODE CATEGORY	FAILURE INDICATOR & STRESS	FAILURE MODE	FAILURE MECHANISM	FAILURE CAUSES
D. Improper Packaging (Continued)	(Same as previous page)		c) Particles in contact area	1) Improper pellet cleaning 2) Improper parts handling
		5. Voids in glass package	a) Insufficient temperature in sealing cycle to complete glass-to-metal seal	1) Test equipment malfunction 2) Operator error
		6. Improper lead assembly	a) Lead detached from slug	1) Undercutting of weld in cleaning and plating operations 2) Improper weld
		7. Improper sealing	a) Device overheated in assembly	1) Equipment malfunction 2) Operator error 3) Improper equipment setup
		8. Improper plating of leads or defective lead construction	a) Leads break off	1) Corrosion 2) Mechanical fatigue at weak spot
		9. Glass package cracked	Glass failure leads to parameter degradations directly associated to this basic effect. a) High R contacts par-tial opens b) High I_R - damage to pellet c) Slug contact to pel-let high V_F d) Leakage in glass crack-I_R increase e) Contaminant introduced thru crack	1) High temperature oxidation of leads causing strains in glass 2) Improper thickness of copper in Dumet leads

FAILURE MODE CHART SILICON PLANAR DIODE.

FAILURE MODE CATEGORY	FAILURE INDICATOR & STRESS	FAILURE MODE	FAILURE MECHANISM	FAILURE CAUSES
E. Improper Measurement Procedure	Drastic or catastrophic shifting of electrical parameters resulting in "open" or "short" category caused by high power surge or mechanicel abuse.	1. Ohmic or resistive current path between anode and cathode slug	a) Significant melting of assembly materials	1) Sufficient resistance heating to produce alloying temperatures 2) Equipment surges 3) Testing anomalies
		2. Mechanical damage	a) Excessive stress on parts	1) Improper fixtures 2) Improper handling

FAILURE MODE CHART SILICON PLANAR DIODE.

FAILURE MODE CATEGORY	FAILURE INDICATOR & STRESS	FAILURE MODE	FAILURE MECHANISM	FAILURE CAUSES
F. Thermal overstress beyond the physical limits of the device	Drastic or catastrophic shifting of electrical parameters resulting in "open" or "short" category caused by high power dissipation stressing.	1. Thermal overload due to diode weakness.	a) Localized heating causing a hot spot and subsequent alloying or diffusion	1) Localized current density 2) Non-uniform doping levels 3) High power dissipation
		2. Thermal overload of runaway of normal diodes due to circuit overload.	a) Excessive heating causing subsequent alloying of materials	1) Sufficient series resistance heating to produce alloying temperatures 2) High power dissipation 3) Extreme current density due to high temperatures 4) Transients and surges in life test racks

2.3 Failure Analysis

The failure analysis studies have been completed for twenty-one of the diodes which failed on the various stress tests. The diode serial numbers, the stress and the failure mode code are all summarized in Table 2. The failure mode code is defined in the Failure Mode Chart (paragraph 2.2).

2.3.1 Type A-2-a Failures

This is the largest category of failures (52.4%). All diodes in this group degraded by a softening of the reverse leakage characteristic after stressing under forward bias and high temperatures. Figure 2 1 shows the voltage-current characteristic of Diode #59 which is typical of this group. The reverse leakage current degradation at low measuring voltages is relatively slight. At increasing voltage levels, the excess leakage current becomes progressively higher. At the high level measuring point of 50 volts, the leakage increase may be as much as several microamperes. Near the avalanche breakdown of the device, leakage may be in the milliampere range. Type A-2-a degradation may be attributed to either surface changes or to bulk diffusion effects.

The surface accumulation mechanism was discussed in detail in the Second Technical Documentary Report[9], and showed that positive ions located in the oxide may diffuse to the silicon-silicon oxide interface on the N side of the diode junction due to the action of the forward bias electric field. This field, extending from the silver button to the silicon beneath it, amounts to approximately 7000V/cm in contrast to the high intensity opposite fields (in the order of 500,000V/cm) which can be produced by reverse biases such as 70 volts. However, mobile positive ions such as the alkali metals

TABLE 2

FAILURE SUMMARY

FAILURE MODE	SERIAL NUMBERS	TEST FAILED	SUB TOTAL	PERCENT CONTRIBUTION
A-2-a	59,60	I_F=50 ma, T_A=100°C	11	52.4
	73,74	50 ma, 150°C		
	61,62,63	100 ma, 100°C		
	72	100 ma, 150°C		
	83,84,85	125 ma, 100°C		
B-2-a	58	I_F=100 ma, T_A=100°C	1	4.8
F-1-a	86,90	I_F=450 ma, V_R= 30V	5	23.8
	87,89	V_R= 30 V, T_A= 150°C		
	88	T_A= 200°C		
F-2-a	57	V_F= 0.2V, T_A= 75°C	4	19.0
	79	I_F= 1 ma, T_A=150°C		
	80	V_R= 30V, T_A=125°		
	82	I_F= 125ma, T_A=100°		
		TOTAL	21	100.0

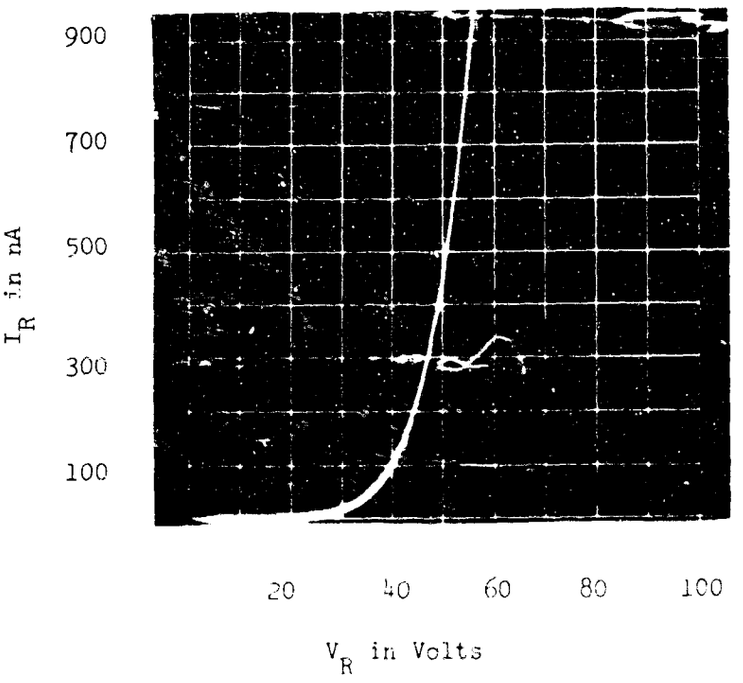


FIGURE 21

REVERSE CHARACTERISTIC CURVE

TRACE OF FAILED DIODE

can be moved and accumulated at the interface even under low intensity fields. A positive oxide accumulation will result in an equal and opposite surface accumulation of conduction electrons in the silicon. This N+ type accumulation will narrow the junction space charge at the surface and may result in non-uniform sites with low voltage avalanche. If accumulation is heavy enough, space charge regions thin enough to support a tunnelling mode of reverse conduction will result.

The bulk diffusion mechanism described by Henning and Miller [10] involves reverse current softening by diffusion of metal from surface contaminants, or contacts, into junction defect sites. The contaminants will precipitate interstitially. Very high fields at the sites of the precipitation will again result in a tunnelling mode of excess current.

2.3.2 Type A-2-a Recovery Tests

Field generated surface space charges described by the first failure mechanism should respond readily to high temperature bakeouts. If mobile ions have been separated by electric fields and high temperature, they should recombine when the external bias separating field is removed and temperature alone is acting. The recombination of oxide ions should produce recovery of the low leakage.

Henning and Miller characterize the reverse softening degradation by diffusion as a temperature activated mechanism which is independent of the source of temperature (whether it originates from a high ambient or from power dissipation in the junction). The implication in this work is that diffusion degraded devices will not recover under bakeout but will remain unchanged or degrade further.

Bakeouts of the failed units were found to have a slow recovery effect. The degree of recovery tends to be complete at the low measuring voltages and is slower and less effective at higher voltage levels. Diodes baked at high temperature for long periods to obtain virtually complete recovery will still have breakdown regions softer than the original characteristics. A summary of the recovery bakeouts performed is shown below:

TABLE 3 - RECOVERY BAKEOUT SUMMARY

Serial Numbers	Bakeouts Temp.	Time	Pellet Ambient	I_R Recovery at 50V	At breakdown
60, 61, 62, 63	200°C	90 Hrs.	glass enclosed	complete	soft
73, 83	200°C	136 Hrs.	glass enclosed	95%	soft
72, 74	200°C	164 Hrs.	Air	80%	soft

The last two diodes were measured and baked in air after removal of the pellets from the glass encapsulation. Air exposed diodes showed no tendency to recover faster than encapsulated diodes. Transistor experience indicates that surface degraded by electro-positive oxide accumulations [11,12] tend t recover more readily in air or oxygen than in nitrogen. Thus the lack of kinetic response in air tends to support a bulk failure mechanism.

To summarize the observations based on bakeout behavior:

1. Reversibility and recovery under bakeout indicates the action of some kind of surface mechanism.
2. The slowness and incompleteness of this recovery suggests, at least, the partial effect of a diffusion mechanism; or it may suggest a surface mechanism caused not by separation of mobile ions in the oxide, but by an increase in density of background positive surface states

such as those normally found in clean, ion free, thermally grown oxides. The surface state increase may be relatively irreversible and may be activated by current flow and temperature rather than by temperature alone.

2.3.3 Reverse Voltage - Current Characteristic Tests

To investigate the nature of the excess current in both Both the forward and reverse directions, plots ot the voltage-current characteristics were made for four A-2-a degraded and undegraded diodes. A comparison was then made between these curves and equation constants reported in the literature. Figure 22 is the log plot of reverse leakage for determining the power constant M in the equation $I_R = K V^M$. Table 4 summarizes the condition of the diodes and the values of M.

TABLE 4

Diode Power Constants

Unit Number	Condition	@V ≤ 15 Volts	@V ≥ 20 Volts
28	Not Degraded	.25	Increasing
29	Not Degraded	.35	Increasing
84	Soft Degraded	1.22	5.2
85	Soft Degraded	0.22	4.8

The low voltage power constant M for three of the devices either approximates the 1/3 value which is expected for reverse leakage from space charge generation in a diffused-graded junction or is somewhat lower for the two devices with higher leakage levels at 10 volts. Low M values at the low voltages are probably surface effects due to space charge influence by the silver button field plate capacitor.

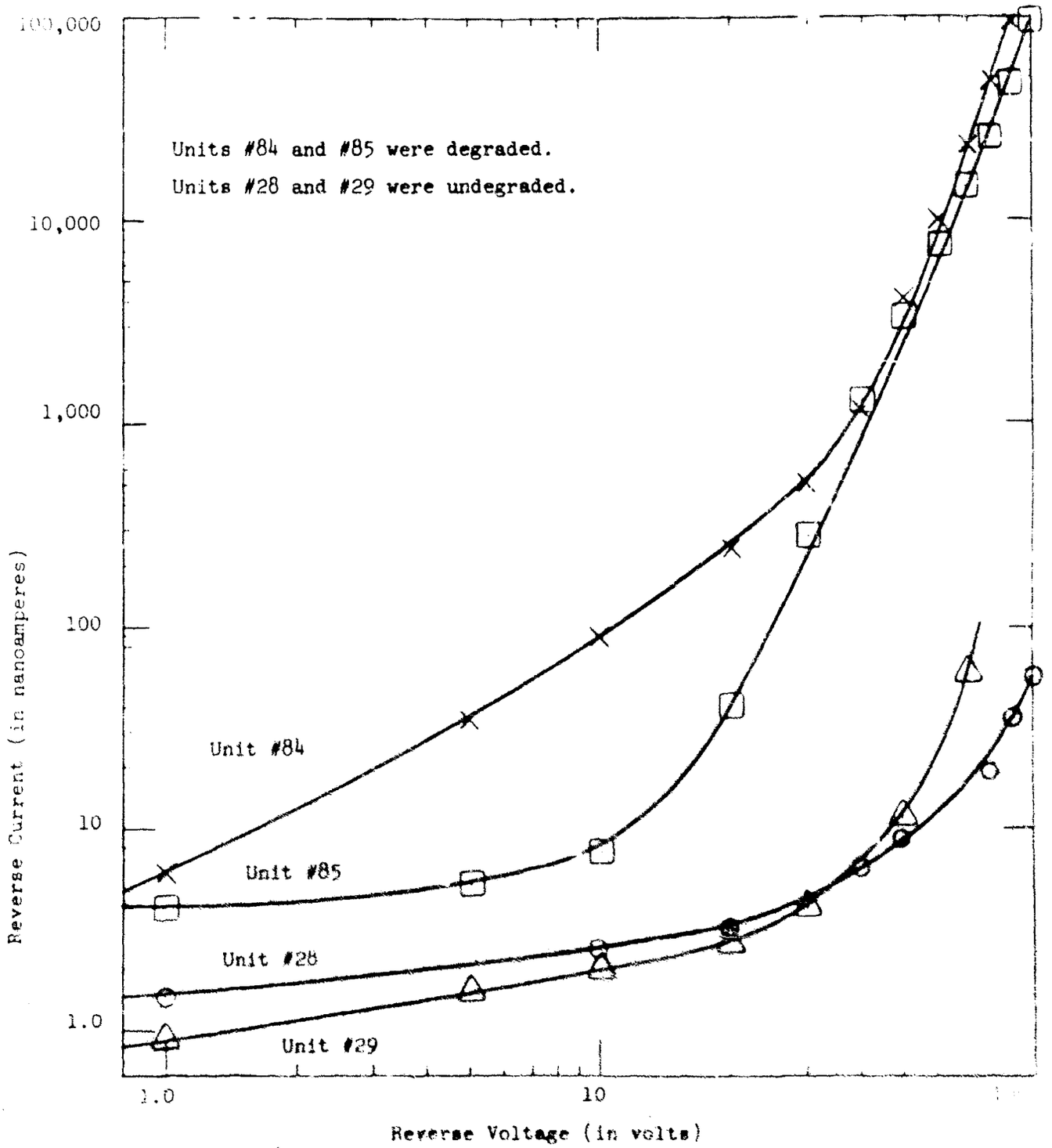


FIGURE 22

REVERSE LEAKAGE COMPARISON FOR
DEGRADED AND UNDEGRADED DIODES

Diode number 84 exhibits a different leakage mode with a large excess current increment increasing as the 1.2 power of voltage. This relation may be representive of a tunnelling mode of a different source from that occurring at higher voltages. An ohmic leakage component (with M=1) may also be responsible for this behavior at low voltages.

Above 20 volts the reverse leakage current increase with voltage, for the non-degraded diodes, follows a rapidly increasing non-saturating pattern which is probably due to multiplication or generation in the high defect density sub-epitaxial region as the space charge region punches into it.

The two degraded devices exhibit large currents at higher voltages far in excess of the normal generation current seen in undegraded diodes. The voltage current relation is approximately $I_R = KV^5$; this being completely consistent with the power law relation reported by Goetzberger and Shockley [13] for tunnel currents generated by high field regions in junctions having metal precipitates.

An extrapolation of this tunnel current to lower voltage levels (2-3 volts) will give an insignificantly small leakage component. Tunnel site generation is thus completely swamped out by space charge generation and other mechanisms active at low voltages.

Measurements made at low temperatures should more clearly define these currents since space charge generation components should drop off much more rapidly than the tunnelling components. Such measurements are being made, but have not been completed at this time.

2.3.4 Forward Current Characteristic Tests

Figure 23 provides a plot of forward current versus bias for the same diodes that were discussed in paragraph 2.3.3. A good straight line fit was obtained on semi-log paper for both degraded and non degraded diodes. The standard forward bias equation of the type $I_F = I_S (e^{\frac{qV}{nKT}} - 1)$ fits both good and degraded diodes. Any power law component due to tunnelling is swamped out by injection. Excess current (which would result in h_{FE} degradation in an emitter junction) is seen in the forward direction for degraded diodes, with no change in the value of n = 2.0. An increase in n is reported for field emission junctions by Henning and Miller. In summary, reverse leakage measurements of softened diode junctions have characteristics associated with tunnelling; this being especially evident at higher voltage measurements. Forward current measurements show excess currents not necessarily associated with tunnelling.

2.3.5 Type F-1-a Failures

A failure pattern common to five diodes (#86 through #90) was noted at 6000 hours for diodes in the long term life test series. These diodes had been stressed as listed below:

86, 90	Rectifying-I_F = 450ma, V_R = 30V, $T_A = 25^\circ$
87, 89	Reverse Bias - $T_A = 150^\circ C$, V_R = 30V
88	Storage - $T_A = 200^\circ C$

After measurement on the automatic readout equipment, all five diodes showed severe reverse leakage current degradation. Figure 24 shows the voltage-current characteristic of unit 86 as a typical example. The reverse leakage current is relatively flat from 0 to 8 volts (5 microamperes) and then sharply

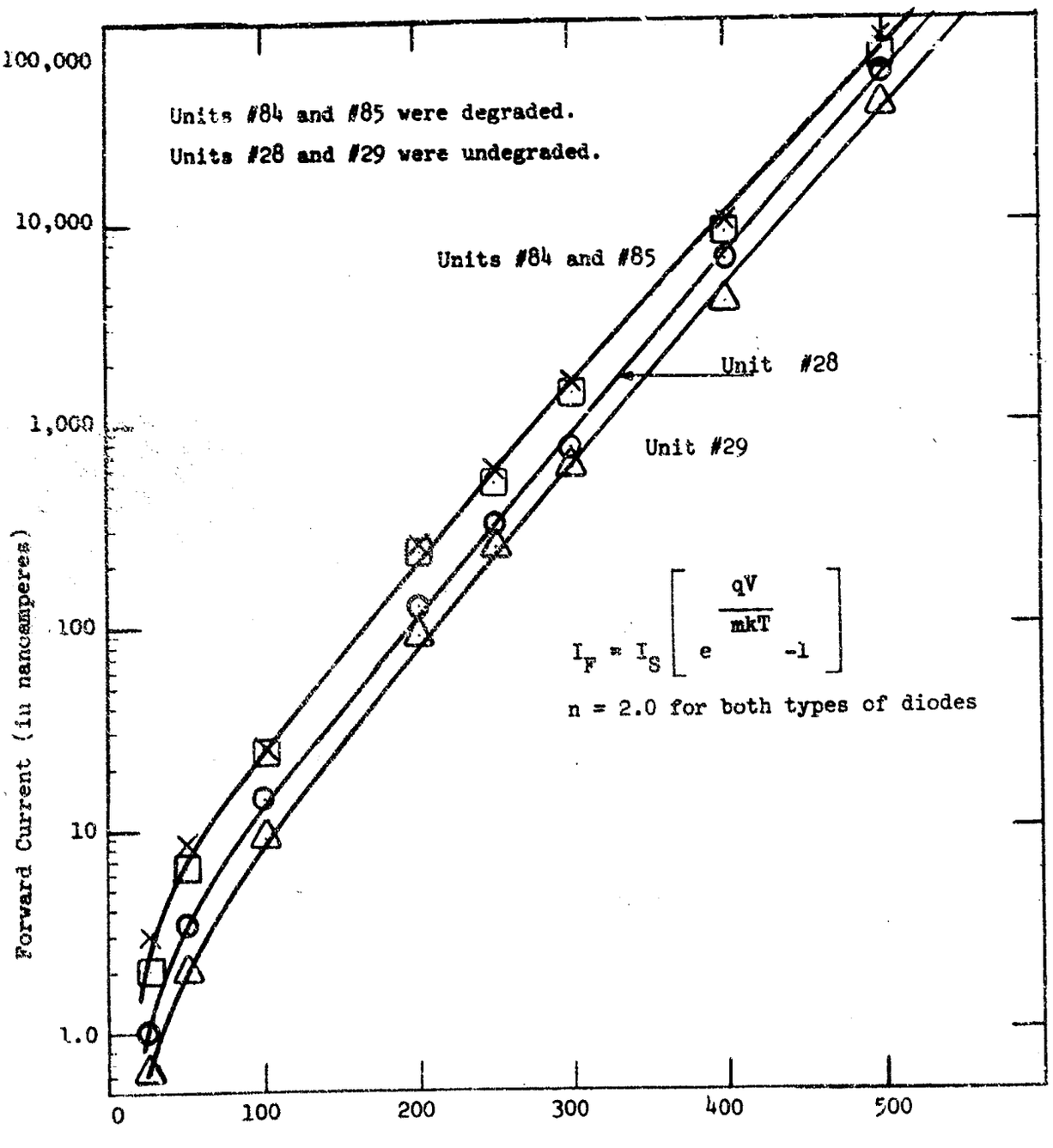


FIGURE 23

FORWARD CURRENT COMPARISON FOR DEGRADED AND UNDEGRADED DIODES

increases to a value of 25 milliamperes at 33 volts, finally tapering off in a negative resistance switchback at high current levels.

This characteristic is identical to that reported for diodes which are pulsed in curve tracer analysis under extreme reverse breakdown conditions, such as 25-35 milliamperes and 140 volts. This is equivalent to a dissipation of 300 milliwatts peak per square mil of junction area. This level of power surge is reported to result in a secondary breakdown type of bulk junction degradation almost identical to the reverse characteristics seen in these diodes. Diodes pulsed at high current levels in the forward direction degrade as dead ohmic shorts in contrast to the observations above.

Examination of the last readout data (6000 hours) shows that normal reverse leakage current readings were obtained initially, significant decreases of about 5% were recorded in the subsequent breakdown voltage readings and some decrease was also noted in the forward voltage drop. The final, repeat check of reverse leakage current at 50V (which is taken to check for measurement transient and anomaly effects) then showed the diodes had severely degraded during measurement; most probably during the breakdown voltage tests.

This fact, combined with the previously noted similarity to diodes overstressed in the breakdown voltage avalanche mode are clear indications that some type of high power transient pulse had occurred during the breakdown voltage measurements.

One element of the data did not allow the assignment of a categorial "non-legitimate" failure cause to these failures. All five failures originated from one particular pellet lot. At the time of test measurement, equal numbers of diodes from six different lots were tested identically in mixed

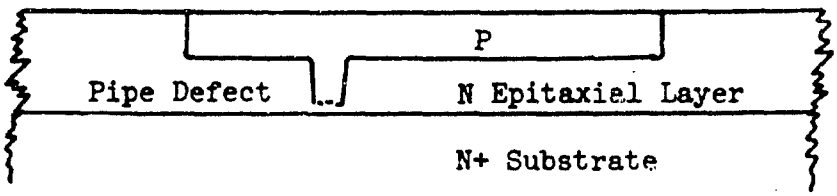
sequences. The transient pulse condition resulted in failures only for the one diode lot. The implication exists therefore, that this diode lot was more susceptible to abusive stresses than other average diodes; perhaps because of non-optimized construction characteristics. On this basis, the failures were assumed to be legitimate with an F-1-a code, and investigations as to the degree of overstress needed to trigger failure were started.

The breakdown voltage measurement circuits have a built-in current limitation, a 100 kilohm resistor in series with each diode being checked. Thus, even if poor or intermittent contact resistances allow the sweep voltage to build up to its maximum value of 700 volts DC, the resulting pulse, when contact is re-established, cannot exceed 6-7 milliamperes. This level is still approximately four times lower than the stress failing a "normal" unit. Diodes with low breakdowns may be suspected to be more susceptible to this failure mode for two reasons:

1. A transient voltage spike will produce a higher current level in the low breakdown diode.
2. A low breakdown device may be one in which the junction is in very close proximity to the sub-epitaxial region. Any destructive spike tending to warp the junction downward will punch into this region more readily. Subsequent sectioning to check on the geometry did not substantiate this explanation.

A statistical compilation of breakdown voltages was made for the six pellet lots. The compiliation showed that the one pellet lot contained the lower breakdown voltages, but the difference in voltage from the other five lots was not significant enough to assign this as the exclusive cause of failure.

Several experimental diodes were fabricated with a variety of button materials and it was determined that the degradation was not related to migration and alloying of contact metal into the junction. The characteristic shape of Figure 24 can be explained by an induced junction defect resulting in current hogging in the defect areas. The sketch shows a cross section of this type of defect.



A defect pipe contacting N+ sub-epitaxial region will explain the low initial breakdown noted (8V), and the resistive saturating characteristic at higher voltages may be due to depletion narrowing of the pipe by the increased voltage.

The possibility of microplasma (defects crossing the junction surface) contribution to the sloping characteristic was explored and eliminated. The junction did not show light emission under reverse drive and bakeouts at high temperature had no effect on the characteristic. Microplasmas will frequently change as surface potentials move in bakeouts.

Diodes #86 was chemically etched to remove all metal from the junction and was then etched in a mild silicon etch designed to preferentially attack defect sites. A tiny defect pit was noted, not more than 4 microns in diameter, which most probably represented the secondary breakdown site - see Figure 25.

Figure 26 is a section taken through the etched junction. It shows an unusually shallow diffusion depth which is contradictory to the expected depth discussed earlier. The junction irregularity seen in Figure 26 may be an [illegible] irregularity in a discoloration site, but does not extend deep enough to

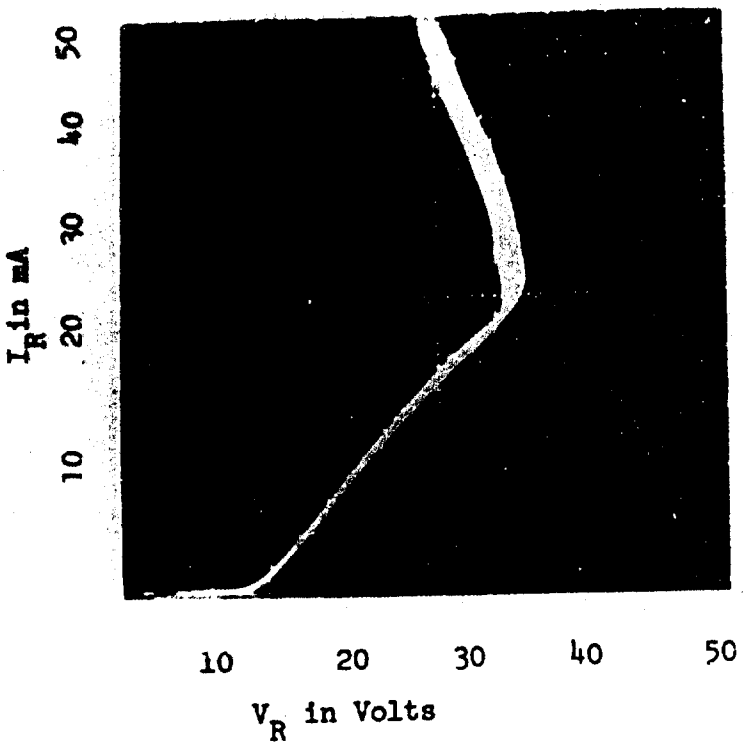


FIGURE 24
CURVE TRACE OF UNSTABLE
NEGATIVE RESISTANCE REGION

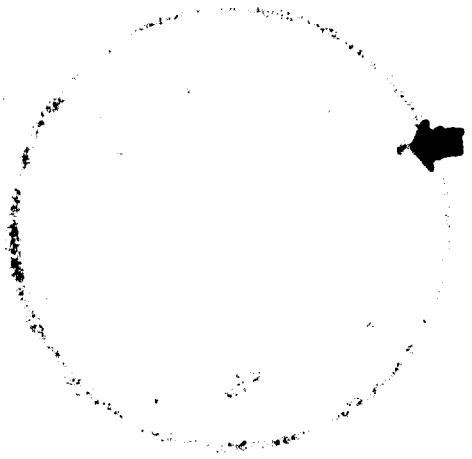


FIGURE 25
PHOTOGRAPH OF ALLOY SPOT

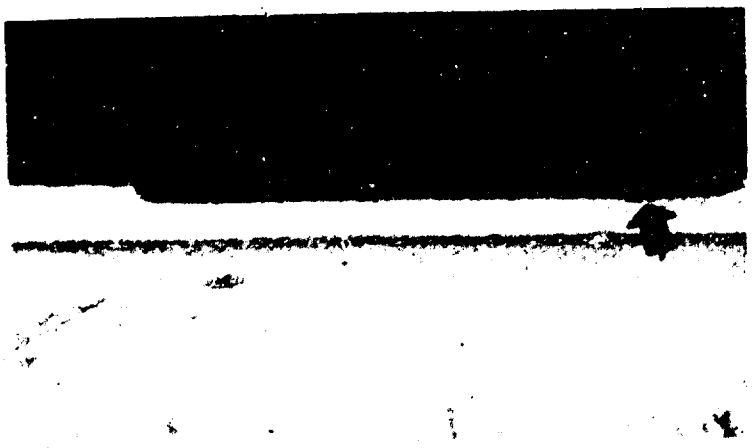


FIGURE 26
PHOTOGRAPH OF CROSS SECTION
THROUGH ALLOY SPOT

be the site of the severe bulk degradation. The magnification of the figure is about 700X and shows a junction depth of 3.7 microns and an epitaxial depth of 10 microns.

At this time, the failed diodes are assumed to have a higher density of defect sites than other diodes which makes them more susceptible to over-stress conditions. Investigations are still in process to measure the power levels required to degrade these diodes.

2.4 Forward Bias Model Building Experiments

The differences in response to forward bias stressing between pellets mounted on TO-18 transistor headers and pellets mounted in the standard glass package has been discussed. The forward bias degradation could be related to metallic contaminants, dislocation density sites in the junction (in which precipitates may form) or ambient conditions. To investigate these areas experimental diodes were assembled and tested. When the pellets were assembled on the transistor headers, some of the anode contacts were made by bonding a gold wire to a non-overlapping aluminum contact. This construction, shown in Figure 27, was used to reduce the amount of contact metal in close proximity to the junction and to eliminate the field effect of the overlapping contact. It was felt that mounting the pellets on TO-18 headers would reduce strains, dislocation and metallic precipitates due to the following factors:

1. The kovar base of the header is closely matched in thermal expansion with the silicon. This should result in lower compressive forces on the pellet in comparison with those obtained in the normal sealing process.
2. The pressure used in assembling glass diodes may introduce plastic deformations at the high assembly temperatures. TO-18 assembly operations are

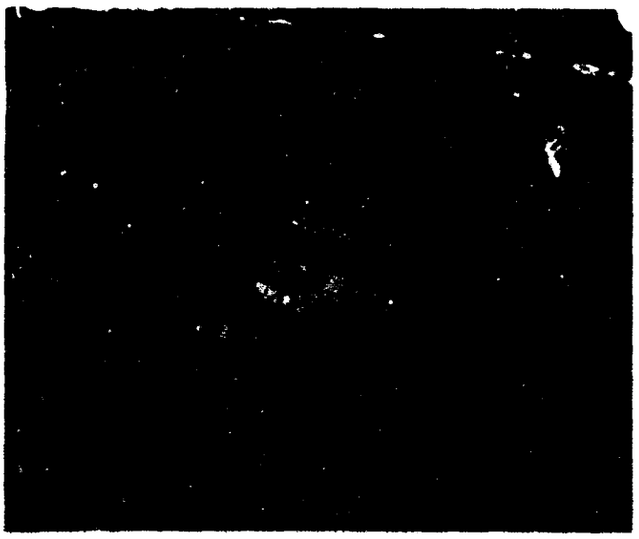


FIGURE 27

PHOTOGRAPH OF DIODE WITH
NON-OVER LAPPING CONTACT

at much lower temperatures.

3. The TO-18 assembly process is peroformed in an ambient free from contaminants, such as glass and borate salts, which are toth mobile and soluble at normal sealing temperatures.

When normal diodes and pellets mounted on TO-18 headers are stressed with the same bias, the TO-18 mounted devices will operate at higher junction temperatures since the thermal conductivity is better in the normal package. Despite the higher junction temperatures, the results of a small scale test showed that the pellets mounted on the TO-18 headers did not degrade significantly while the normally mounted devices degraded at the previously observed rates. The test results are summarized in Table 5.

TABLE 5

Forward Bias Test - TO-18 And DHD Mounted Pellets

Pellet	Package	Number Tested	I_F	T_J At T_A = 125°C	I_R Increase at 50 V
Aluminized	TO-18	6	125 mA	223°C	0
Silver Dot	TO-18	8	115 mA	212°C	1 at 1.8X
Silver Dot	DHD	8	115 mA	166°C	1 at 1.4X
					1 at 2X
					1 at 5X
					1 at 7X
					1 at 65X

In a second experiment, a group of pellets were removed from the glass package and were remounted on TO-18 headers with low temperature gold-antimony preforms. The anode contact was made by thermocompression bonding a gold wire to the pellet. Part of the remounted pellets were left uncapped (air ambient) and part were capped (no air ambient). All of the devices, plus some glass mounted controls, were subjected to a forward current of 100 milliamperes, is an ambient temperature of 100°C, for one week. The reverse leakage current response, at 20 volts, is plotted in Figure 28; and, 50 volts, is plotted in Figure 29. The data show:

1. The remounted pellets are better than the control diodes, but not to a significant amount.
2. Three of the pellets that were remounted, and exposed to air, degraded approximately the same amount as the general population.
3. The entire lot of devices, both experimental units and controls, exhibited high initial reverse leakage currents and showed more degradation than average diodes.

The third experiment utilized the same mounting techniques employed in the second experiment. However, the pellets had not been mounted in glass package prior to the experiment. Once again, part of the pellets were left uncapped (air ambient), part were capped (no air ambient), and part were mounted in glass packages. The same stress conditions and time were used and the 20 volt response is shown in Figure 30 and the 50 volt response is shown in Figure 31. For this set of tests, the data show:

1. The pellets mounted on TO-18 headers showed approximately the same degradation whether the pellets were in an air or a nitrogen ambient.
2. At the 50 volt level, the worst degradation for the TO-18 mounted pellets

was 4X. Over half of the normally mounted pellets showed greater degradation than 4X.

Figure 32 shows the results of the last experiment. Two lots of pellets, from the program pellet bank, were sampled, mounted on TO-18 headers, and sealed in nitrogen or left uncapped. Once again, no significant differences in the degradation were noted for the two types of ambient.

All of these experiments led to the conclusion that oxygen was not of primary significance in preventing the reverse voltage-current characteristic from softening under a large forward current stress. These results, which are in contrast to much of the literature, also led to the conclusion that the temperature and pressure in the sealing process are the primary influence for the forward bias failures. These investigations are being continued.

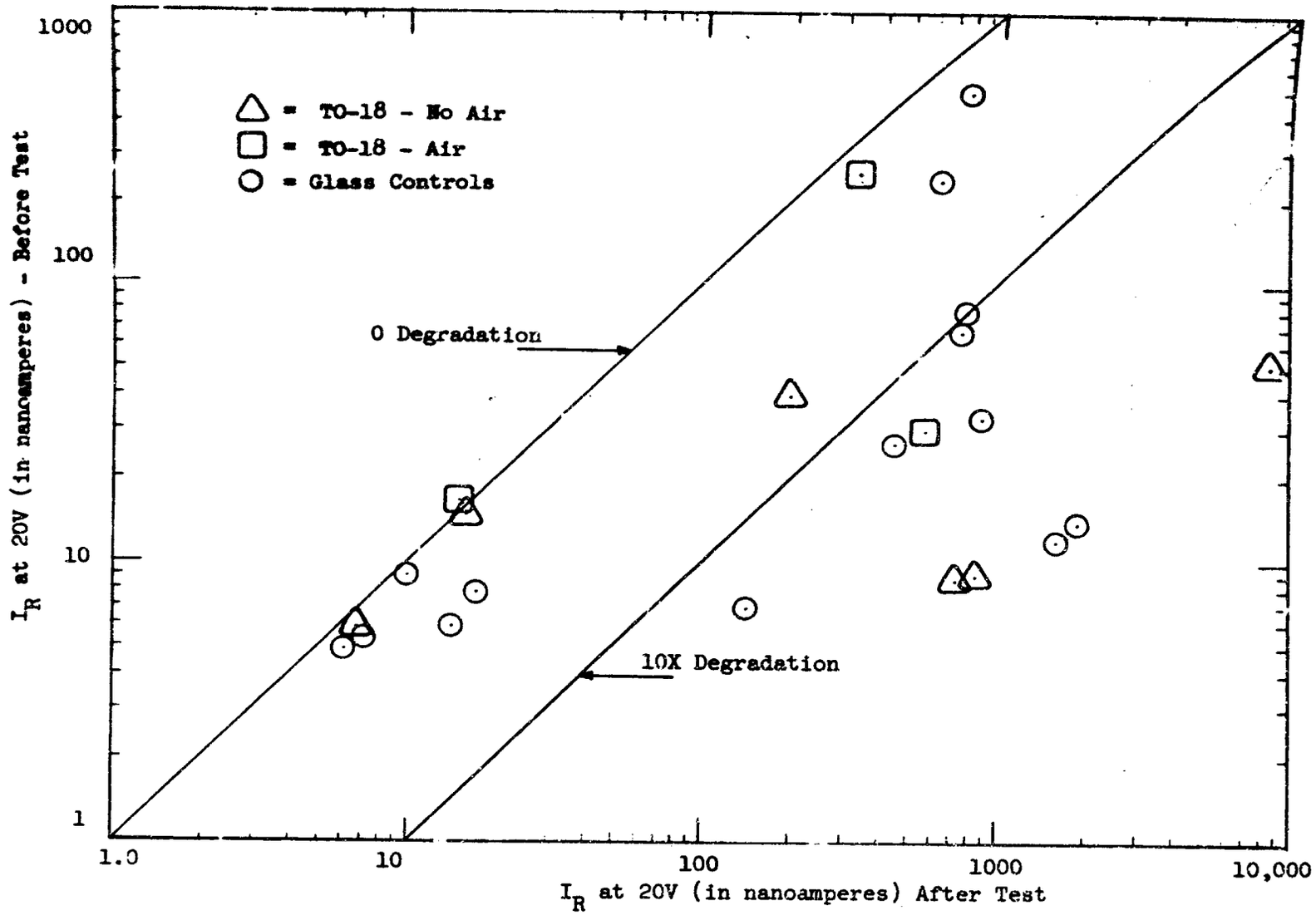


FIGURE 28

REMOUNTED PELLETS - 20 VOLT I_R

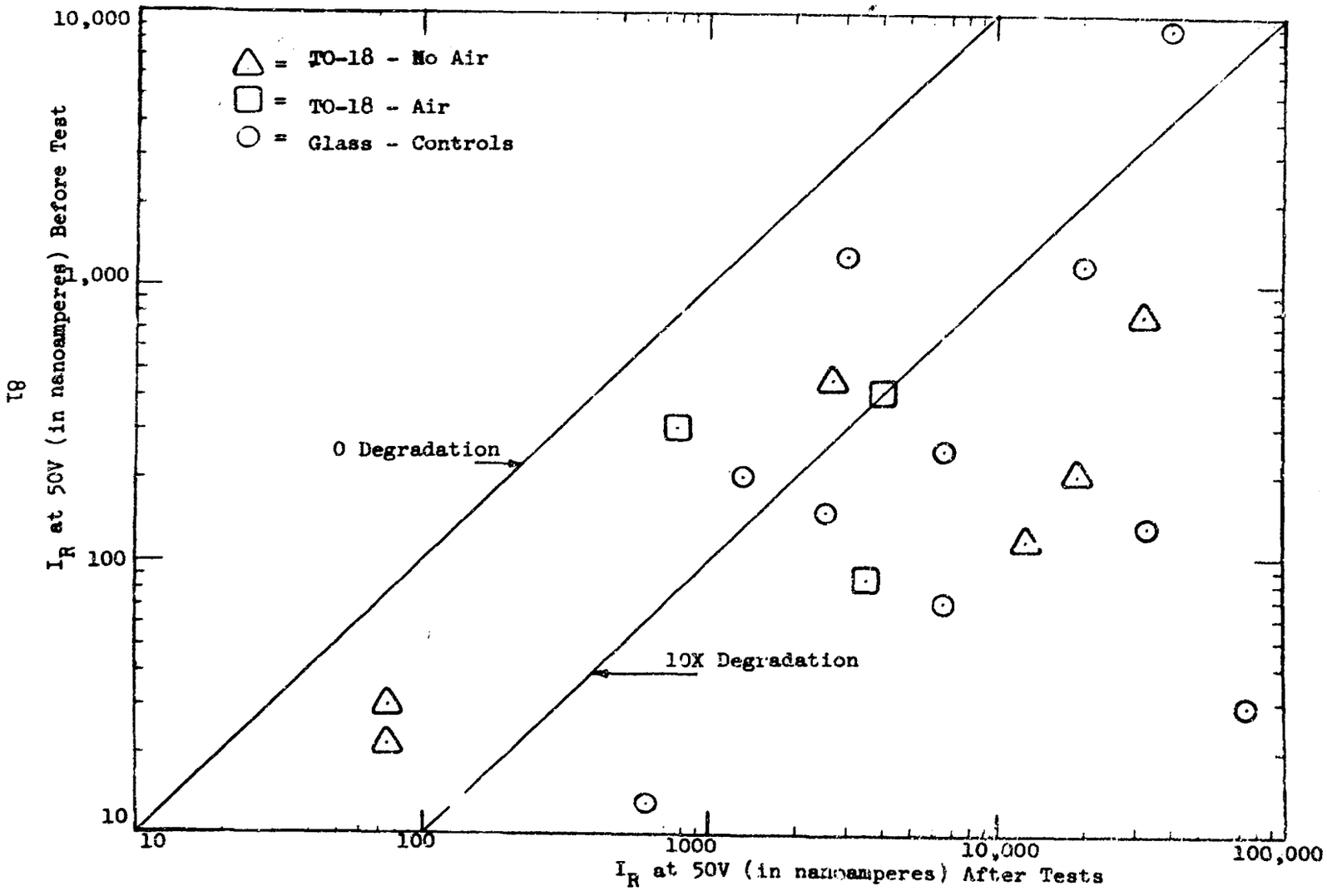


FIGURE 29

REMOUNTED PELLETS - 50 VOLT I_R

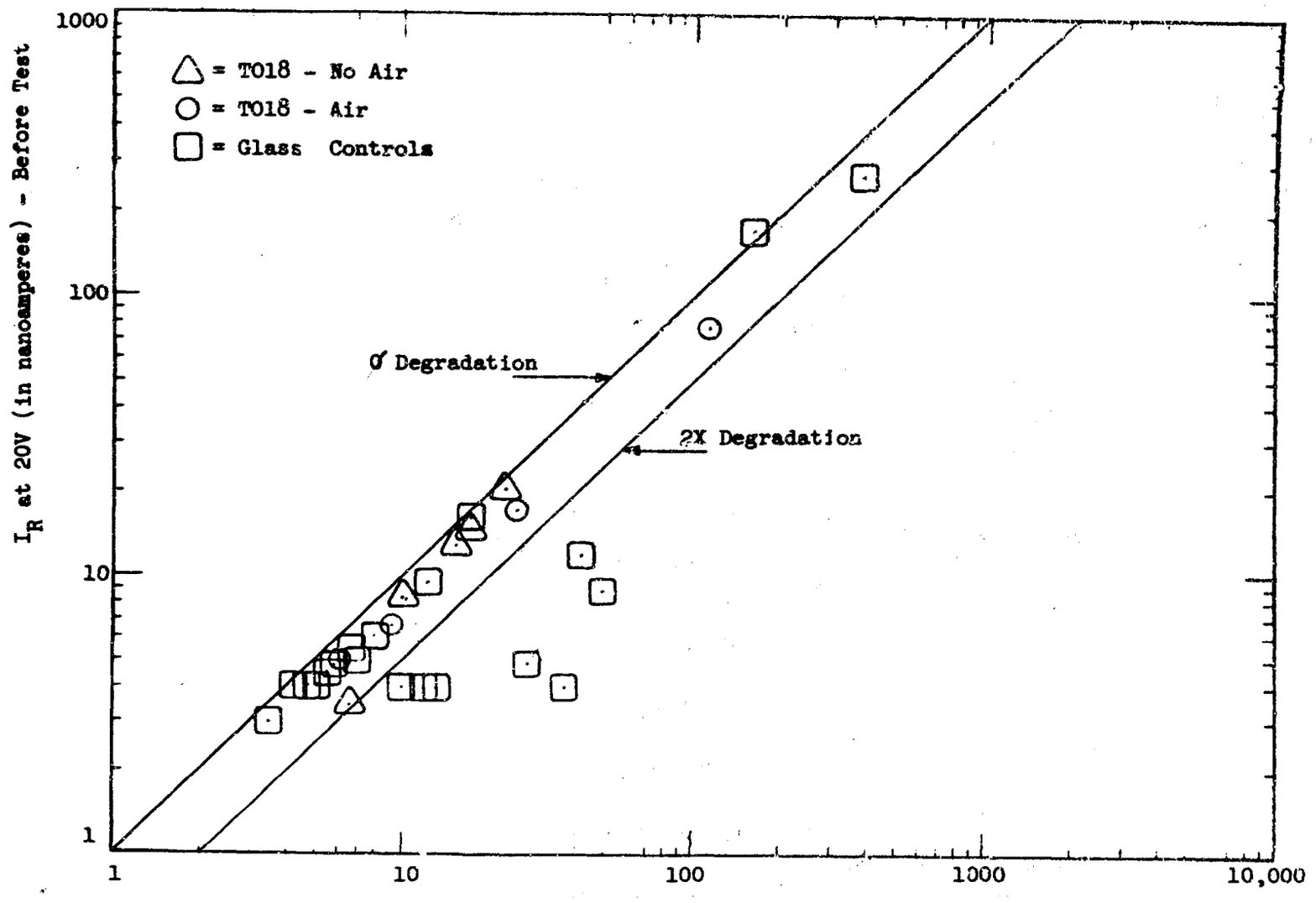


FIGURE 30

UNSTRESSED PELLETS - 20 VOLT I_R

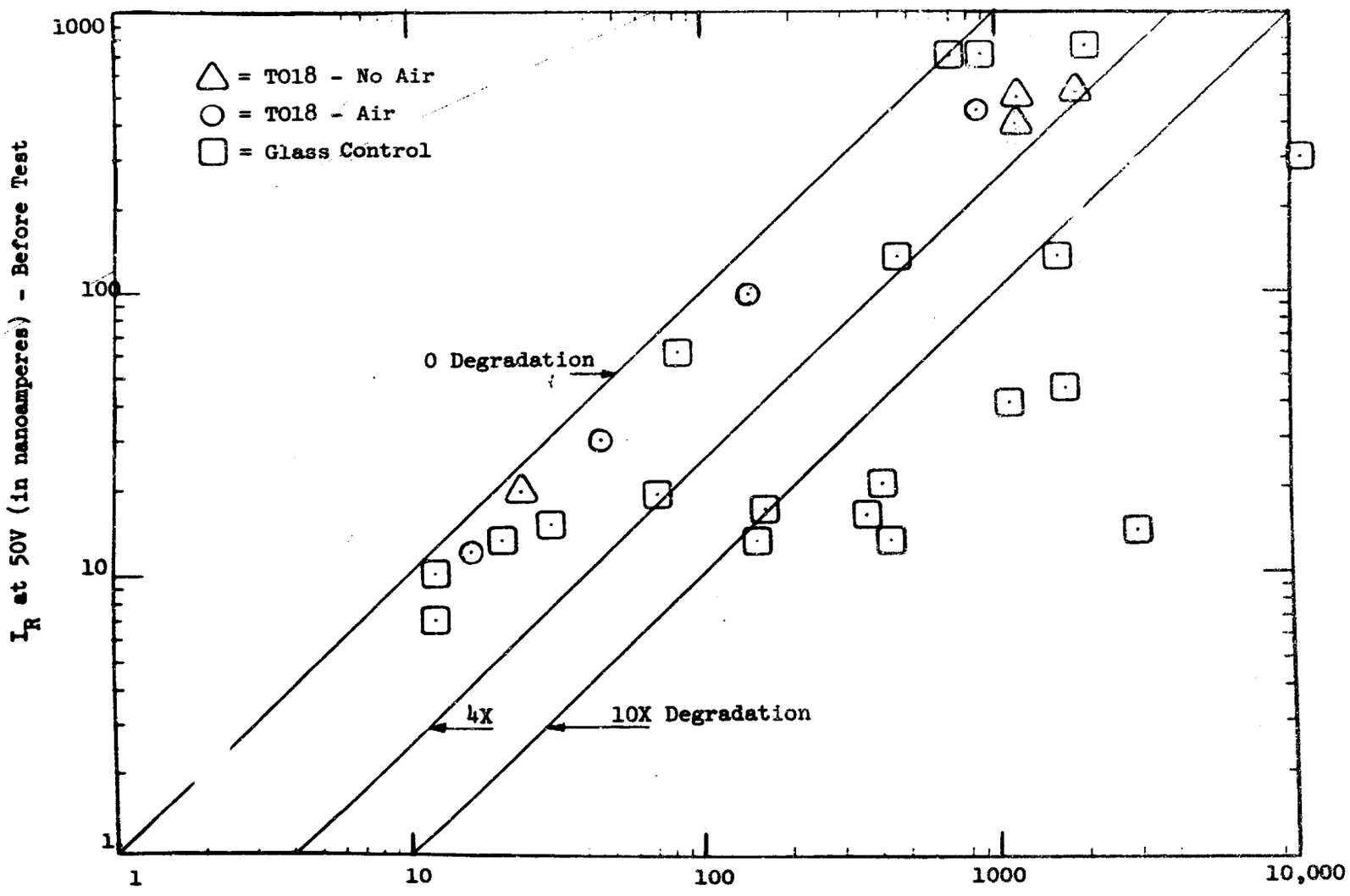


FIGURE 31

UNSTRESSED PELLETS -50 VOLT I_R

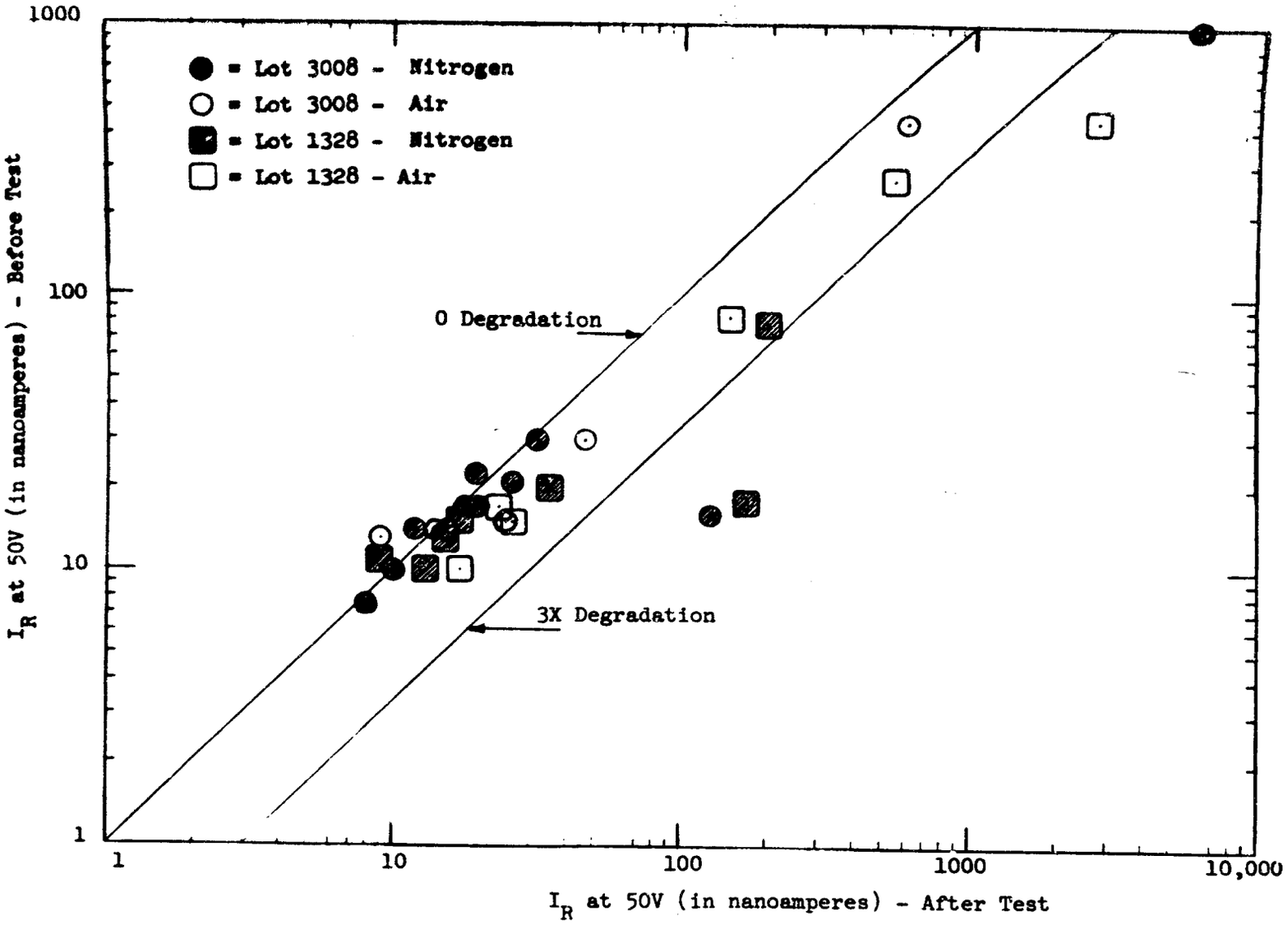


FIGURE 32

PROGRAM PELLETS - 50 VOLT I_R

SECTION 3

MODEL TEST PLANS

3.1 Step Stress Testing

The problems associated with conducting electrical stress tests at very high temperatures required advances in the state-of-the-art. Workable solutions were found, the high temperature test cards have been delivered and the 175°C tests have been started. The 200°C tests will be completed in the near future. The conclusions drawn from the information that has been collected are discussed in Section 4.

3.2 Deterministic Model Test Plan

The Deterministic Model tests will all consist of stress-in-time tests as contrasted with the step-stress tests that have been conducted to date. The change in the form of the tests will enable the most accurate determination of acceleration factors and rate constants of the degradation equations. The test plan will be conducted in two phases; the first phase will utilize diodes from the pellet lots that were established for the program, and the second phase will use diodes with controlled manufacturing process variations. The second phase will be based on the results of the first phase and may be less complex.

The complete test matrix for the Deterministic Model Test Plan is shown in Figure 33. The portion of the test plan for the Reverse Bias model has been discussed in some detail in earlier reports, and is reviewed in Section 4. The portion of the test plan for the Forward Bias model will be conducted first, and is more extensive, since more information is needed to complete this model.

It is expected that some reactions to the stresses will occur quite rapidly. In order to obtain the requisite data, the electrical parameters will be read at 0, 5, 20, 100, 200, 500 and 1000 hours. Some portions of the test matrix may be terminated before the 1000 hour point, if the response to the stresses indicates the advisability of such a step. Based on the results of the step-stress tests, the electrical parameters that will be monitored have been changed slightly, and are listed below:

1. Breakdown Voltage (BV) at 5 and 100 microamperes,
2. Reverse Leakage Current (I_R) at 15, 30, 40, 50, 60 and 70 volts,
3. Forward Voltage Drop (V_F) at 1,100 and 500 milliamperes,
4. Stored Charge (Q_S) at 10 milliamperes,
5. Thermal Resistance (θ_{JC}) at 300 milliamperes (will be read at the beginning and at the end of the test program),
6. Capacity (C_O) at a frequency and bias to be determined.

The shape of the reverse voltage-current characteristic is quite important and it was decided to monitor this shape in the Deterministic Model test plan. An X-Y plotter was used to record the reverse voltage curve shape for all of the diodes that will be tested. At the completion of the test stress, or at the time the unit is removed from test, the curve shape will be recorded again. This will permit an accurate determination of the change in the curve shape. Potential changes in the curve shape will be monitored by the increased number of breakdown voltage and leakage current measurements.

After the reverse characteristic was recorded, several diodes were selected for a capacity investigation. These units are being checked at a variety of bias conditions and frequencies, and the results of the study will determine the measurement conditions for the test plan.

The first pellet lots, with controlled process variations, are rapidly approaching the point of being assembled into complete diodes. The process variations include the extremes of the wafer resistivity range and the oxide thickness range. Varying values of sealing temperature and pressure will be used in the assembly process. It is also planned to measure the junction diameter, button size and junction depth after these devices have been tested. It is anticipated that these variations will provide the necessary information to complete the Deterministic Model and to start structuring the Probabilistic Model.

FIGURE 33

DETERMINISTIC MODEL TEST PLAN

CONSTANT STRESS-IN-TIME

STRESS BIAS	STRESS TEMPERATURE (°C)				
	25	75	125	175	225
I_F = 300 mA	X	X	X	X	
I_F = 200 mA	X	X	X	X	
I_F = 100 mA	X	X	X	X	
I_F = 50 mA		X	X	X	Y
V_R = 75 V		X	X	X	
V_R = 50 V		X	X	X	Y
V_R = 30 V			X	X	Y
V_R = 15 V			X	X	Y

Parameters will be read at: 0,5,20,100,200,500 and 1000 hours.

X = Tests that will be run with 3 diodes from each diffusion lot, 18 diodes per cell.

Y = Tests that will be run if the data from the other tests shows that the high stresses are needed.

SECTION 4

DIODE STRESS TEST RESULTS

4.1 Temperature and Reverse Bias

A Deterministic Model relating diode degradation with the stress variables has been constructed, based on the current results of the step stress and long term, constant stress-in-time data analyses. The model is shown in Figure 34. The stress variables that are explicit in the model are the reverse voltage, V_S, and the time on stress, t_s. The stress variable of temperature is implicit in the model and is related to t_o, the time constant of the degradation mechanism. The dependence of t_o on T_S takes the form of Arrhenius relationship. The temperature, T_M, and electrical bias, V_M, at which the degradation is measured are also implicit in this model.

The detailed breakdown of the model depicted in Figure 34 also indicates explicitly and implicitly those process variables that are expected to influence the degradation. Thus, the Deterministic Model relating the arithmetic increase of leakage current, ΔI, to stress is:

$$I = KV_S^4 \quad (1-e^{-t_s/t_o})$$

where K is a function of the geometry processing variables and measurement conditions, for which a "typical" value can be assumed. The Deterministic Model could be viewed as a mathematical representation of "typical" device behavior relating the change in electrical characteristics with stress. Such models, when shown to be adequate, are useful, for prediction and estimation of degradation; further, the models are extremely useful for ob-

TEMPERATURE AND REVERSE BIAS DEGRADATION MODEL

$$\Delta I = \frac{en}{2\tau} f(V_M) \left(A_c\right) \frac{1}{\left(t_M\right)} \left[\frac{K \epsilon_0 V_S}{\left(d\right)} \left(1 - e^{-t_s/t_o} \right) \right] = \Delta I_S \left(1 - e^{-t_s/t_o}\right)$$

Subscript M refers to Measurement Variables.

Subscript S refers to Stress Variables.

EXPECTED VALUES OF PROCESS VARIABLES (CIRCLED ABOVE)

$\tau = 10^{-8}$ sec. carrier lifetime

$A_C = 2.51 \times 10^{-4}$ cm^2 area underneath silver contact less diffused junction area

$N_D = 10^{15}$ cm^{-3} effective density of donors for n silicon

$d = 1.3 \times 10^{-4}$ cm oxide thickness

CONSTANTS

$e = 1.6 \times 10^{-19}$ coulomb electron charge

$K = 4$ dielectric constant for SiO_2

$\epsilon_0 = 8.842 \times 10^{-14}$ coulombs volt^{-1} cm^{-1} permitivity for free space

$f(V_M) = 1$ for $V_M > 10V$

$n_i = 1.6 \times 10^{10}$ cm^{-3} intrinsic free carrier concentration @ 300°K

I_S NANOAMP / t_0 Hours

Estimates from the Step Stress Tests.

STRESS TEMP. T_M	75°C	100°C	125°C	150°C
25V	1.15 / 2100	11.5 / 988	11.5 / 305	11.5 / 97
30V	16 / 2100	16 / 988	16 / 305	16 / 97
50V	27 / 2100	27 / 988	27 / 305	27 / 97
70V	54 / 2100	54 / 988	54 / 305	54 / 97

FIGURE 34

taining answers to questions relating to acceleration factors, burn-in and device specifications. As the program study progresses, a proper evaluation will be made of the effect of device-to-device variations (inherent in the K factor) on device degradation. The Deterministic Model will then evolve into the more realistic Probabilistic Model.

It should be realized that the development of the Deterministic Model is subject to restrictions. That is, the model was developed for a particular diode geometry and processing and was shown to hold over a region of stress variables. The model shown in Figure 34 was developed for the stress region up to 150°C temperature and 70 volts reverse bias. Preliminary fixed stress testing at 200°C shows a non-saturating effect of degradation which deviates from the degradation model. Thus, the model will be modified for the region of increased stress. With the completion of the constant stress test plan design (Figure 33) for the second year effort, the Deterministic Model will be verified, refined and modified. The model is plotted on linear scales in Figure 35; the linear fit on semi-log paper is shown in Figure 36. The table included with Figure 34 shows the estimation of maximum degradation, ΔI_S, and the time constant, t_o based on the analysis of data from the step-stress testing. These values will be refined in the analysis of the constant stress-in-time matrix.

When the degradation mechanism is established, the step-stress test data can be utilized to obtain first estimates of t_o for different T_S values, and to obtain ΔI_S for different V_S values. As an example, the calculations are performed for the temperature step-stress test in which V_R = 70 volts.

Step 1 - Estimate the expected value of ΔI_S from the final incremental leakage data obtained after the 150°C step (since the time constant

is less than 100 hours at this temperature level, this would be a reasonable estimate) I_S = 54 nanoamperes. The estimated value of 54 nA is inserted into the equation below, as is the 4 nA average leakage shift observed after 168 hours at 75°C (the first step in the temperature step stress).

$$\Delta I_1 = \Delta I_S \left(1 - e^{-168/t_{o1}}\right)$$

$$4 = 54 \left(1 - e^{-168/t_o}\right)$$

and solving for t_o gives

t_{o1} = 2100 hours.

Step 2 - Estimate the "equivalent" stress time, t_s', for 100°C, which is the second step of the temperature stress.

Estimation of t_o for 100°C must take into account the previous 168 hour stress at 75°C. Thus, the 4 nA shift that was actually observed must be related to a reduced time, t_s', on the higher 100°C stress.

$$\Delta I_1 = \Delta I_S \left(1 - e^{-t_s'/t_{o2}}\right)$$

$$4 = 54 \left(1 - e^{-t_s'/t_{o2}}\right)$$

and solving for t_s' gives

$t_s' = .08 t_{o2} + 166$, where t_{o2} is the time constant associated with 100°C.

Step 3 - Estimate t_{o2} for T_S = 100°C

Using the observed average leakage shift, ΔI_2, after the 100°C step, an estimate for t_{o2} is obtained as follows:

$$\Delta I_2 = 54 \left(1 - e^{-t's/t_{o2}}\right)$$

$$1 = 54 \left(1 - e^{-(.08\, t_{o2} + 168)/t_{o2}}\right)$$

and solving for t_{o2} gives

$t_{o2} = 988$ hours

Step 4 - Estimate "equivalent" stress time t_s" at $T_S = 125^{\circ}C$, (the third step in the temperature stress sequence). In a similar fashion to Step 2, the 12 nA shift observed after $100^{\circ}C$ is equivalent to a reduced time, t_s", on $125^{\circ}C$ of $t_s" = 0.25\, t_o + 168$ (neglecting the second order effect of the previous 168 hours at $75^{\circ}C$).

Step 5 - Estimate t_{o3} for $T_S = 125^{\circ}C$. Using the observed average leakage shift of 30 nA, ΔI_3, after the $125^{\circ}C$ step, t_{o3} is estimated in a similar fashion to Step 3.

$$\Delta I_3 = 54 \left(1 - e^{-(.25\, t_o + 168)/t_o}\right)$$

and solving for t_{o3} gives

$t_{o3} = 305$ Hours.

The time for the $150^{\circ}C$ step, t_{o4}, would be approximately 100 hours, which compares favorably with the preliminary estimate of 50 hours from the constant stress-in-time testing. Fitting these estimated values of t_o to the Arrhenius relationship, $t_o = e^{-E_A/KT}$, and equating E_A/KT to the slope of the line (K is Boltman's constant), gives a value of E_A approximately equal to 0.62ev. Applying these estimated time constants to the other temperature step stress cells gave reasonable correlation between the observed and calculated leakage current shifts.

The fit of mean leakage current shift on a recriprocal absolute temperature

scale based on the results of the step stress testing is shown in Figure 37. The actual I_R movement at two measurement bias voltages, after each temperature step stress readout is in Figure 38. Figures 39 and 40 support the assumption of linearity of degradation (ΔI) versus stress voltage (V_S) as dictated by the model.

LEAKAGE CURRENT DEGRADATION IN TIME FOR THE TEMPERATURE AND REVERSE BIAS MODEL $\Delta I = \Delta I_S (1 - e^{-t_s/t_o})$

where ΔI is arithmetic shift of Leakage Current, I_R
ΔI_S is maximum shift for a given Stress Voltage
V_S is Stress Voltage
t_s is time under stress
t_o is time constant (time at which $0.63\Delta I_S$ is achieved).

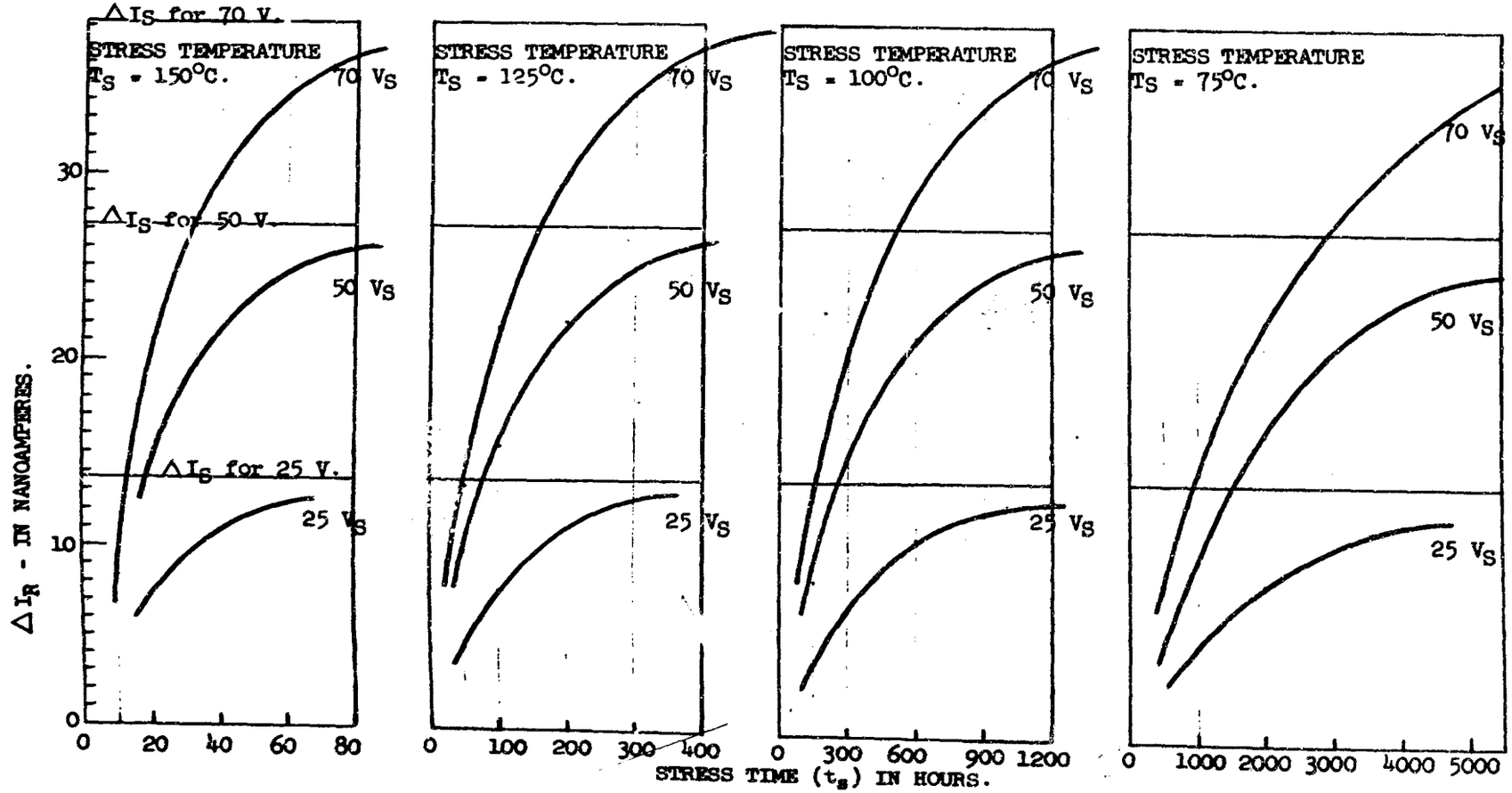


FIGURE 35

LEAKAGE CURRENT DEGRADATION IN TIME FOR THE TEMPERATURE AND REVERSE BIAS (V_R) MODEL FOR STRESS TEMPERATURE 75°C.

DEGRADATION MODEL; $\Delta I = \Delta I_S (1 - e^{-t_s/t_o})$

where ΔI is arithmetic shift of leakage current I_R
ΔI_S is maximum shift (at saturation) - function of stress voltage V_R, measurement temperature, and process and design factors
t_s is time under stress
t_o is time constant (time at which 0.63 ΔI_S is acnieved).

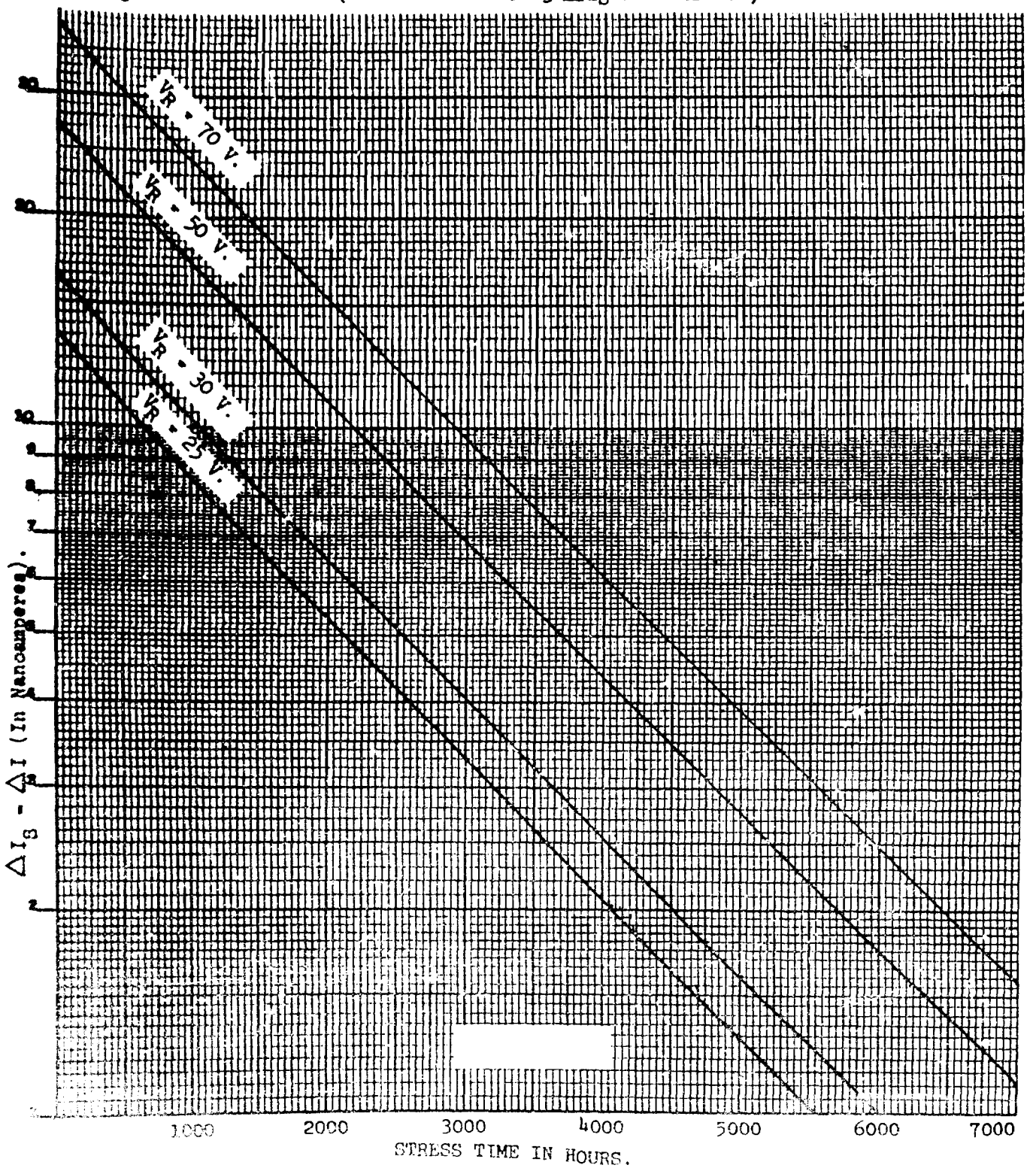


FIGURE 36

MEAN I_R SHIFT ($\overline{\Delta I}$) vs. TEMPERATURE ON TEMPERATURE STEP STRESS WITH FIXED REVERSE BIAS VOLTAGE.

V_S = Reverse Bias Stress Voltage. V_M = Measurement Bias Voltage = 50 V.

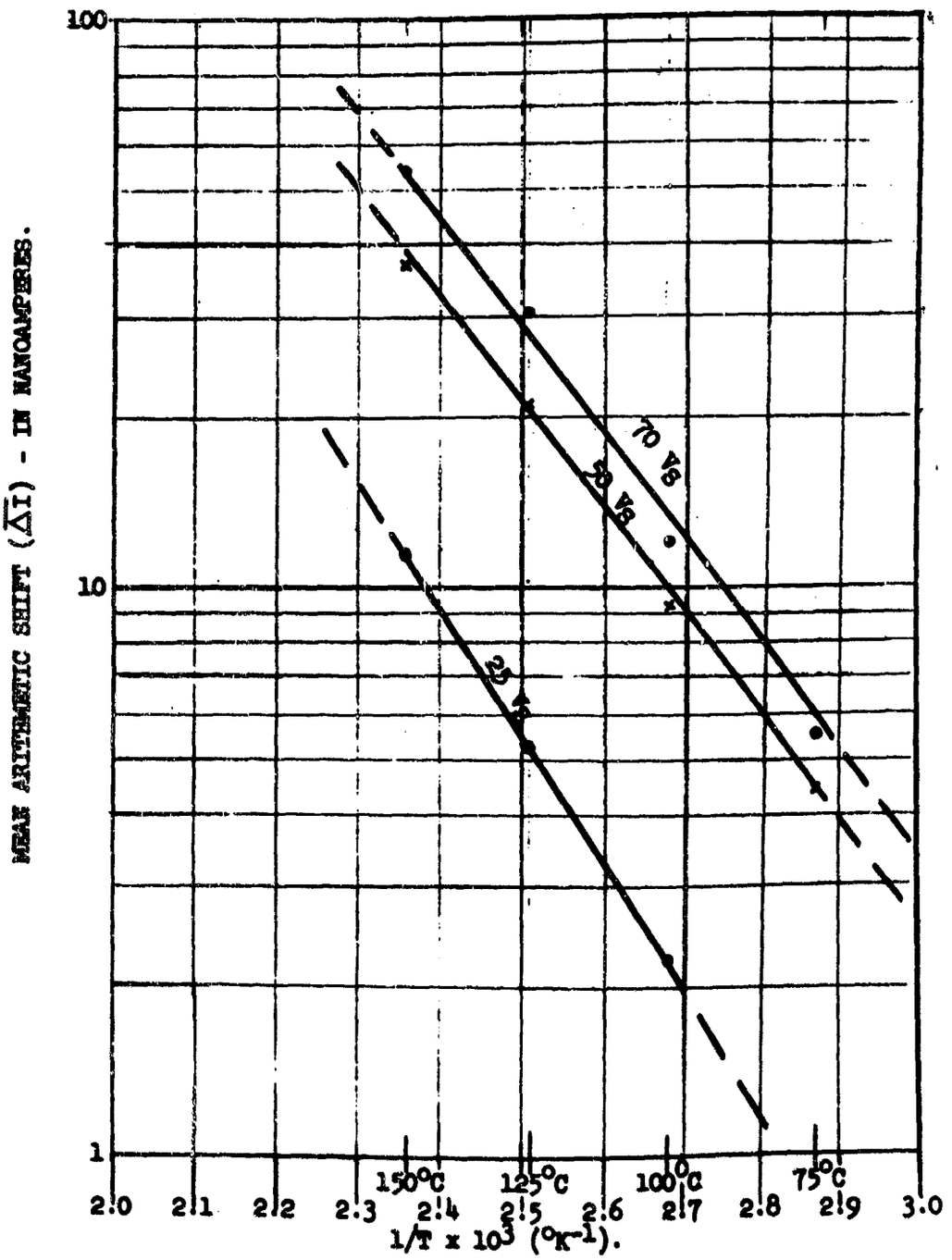


FIGURE 37

MEDIAN I_R vs. TEMPERATURE ON TEMPERATURE STEP STRESS WITH FIXED REVERSE BIAS VOLTAGE. (Stress Cells 16, 17, 18).

V_S = Reverse Bias Stress Voltage. V_M = Measurement Bias Voltage.

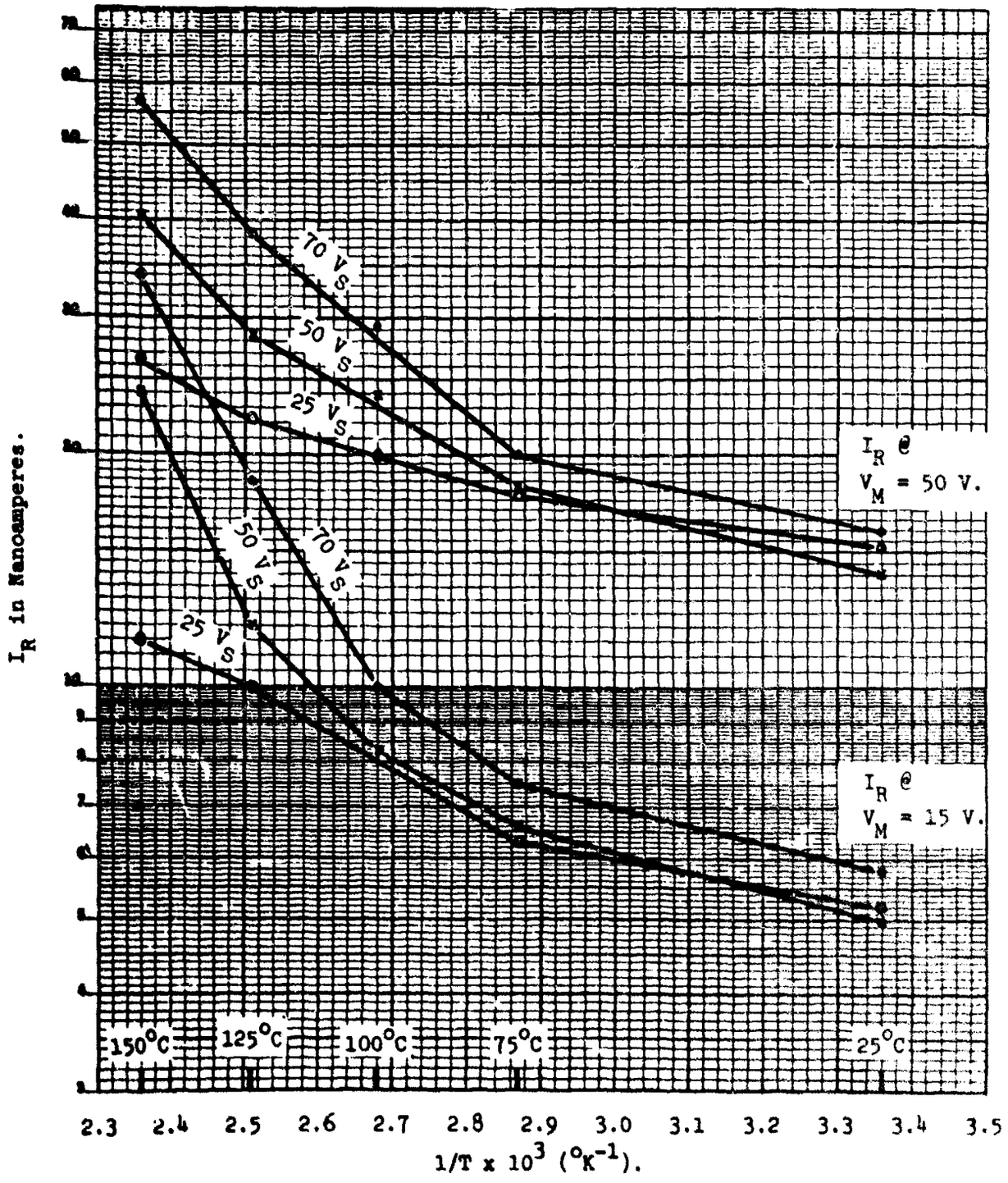


FIGURE 38

APPROXIMATE LINEAR VOLTAGE DEPENDENCE ON
HIGH TEMPERATURE AND REVERSE BIAS TESTS.

REVERSE VOLTAGE IN VOLTS → / TEMPERATURE IN DEGREES C ↓	MEDIAN ARITHMETIC SHIFT IN NANOAMPERES			RATIO OF 70 V. DEGRADATION TO 50 V. DEGRADATION
	25 V.	50 V.	70 V.	
75°C	———	1.7 nA.	2.3 nA.	1.35 X
100°C	———	5.0 nA.	9.6 nA.	1.92 X
125°C	———	14.0 nA.	20.0 nA.	1.43 X
150°C	10.0 nA.	21.0 nA.	37.0 nA.	1.76 X

FIGURE 39

I_R SHIFT ($\Delta\overline{I}$) vs. REVERSE VOLTAGE ON VOLTAGE STEP STRESS WITH FIXED TEMPERATURE (125°C.) (Stress Cell 15).

V_R = Reverse Bias Stress Voltage. V_M = Measurement Bias Voltage

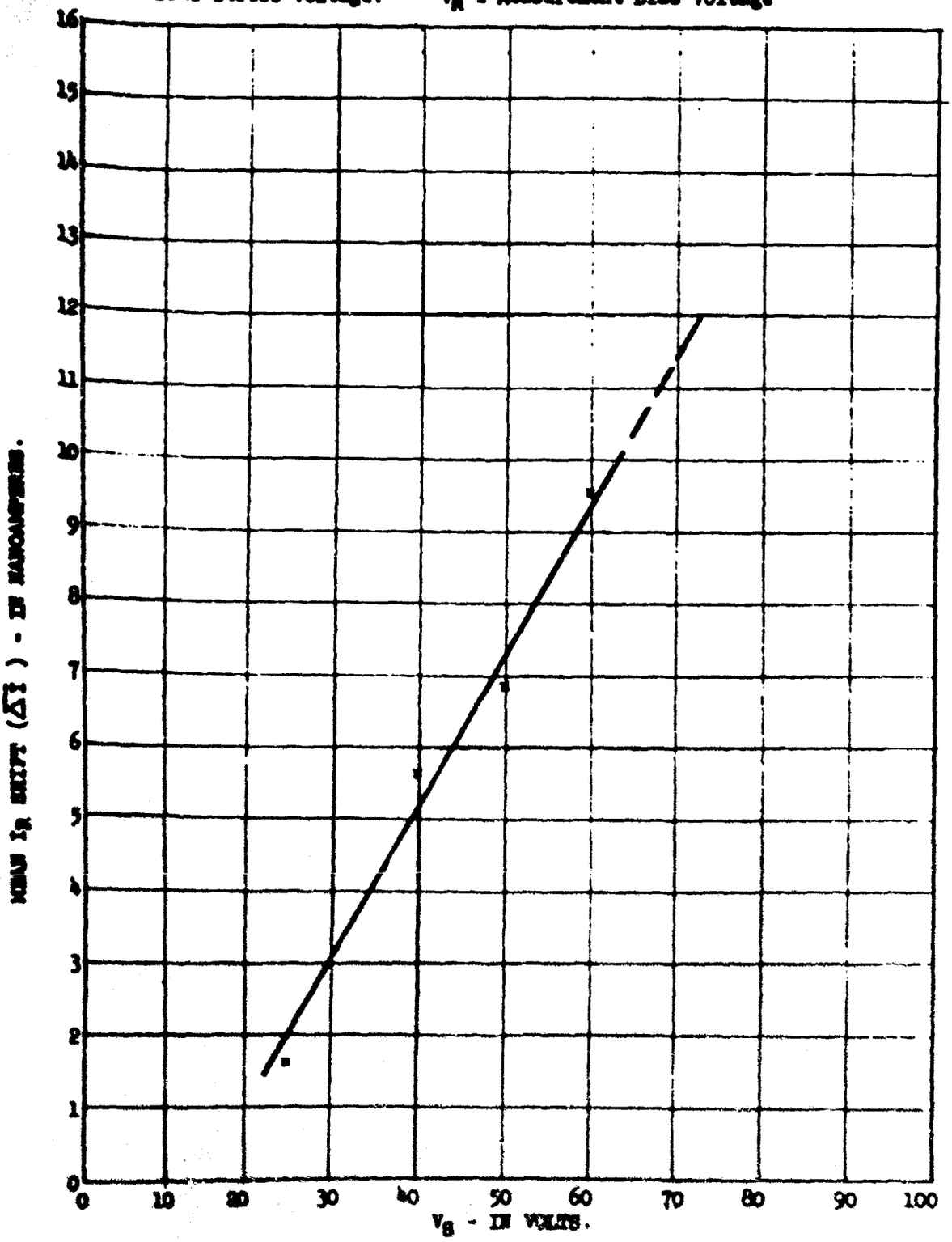


FIGURE 40

4.2 Temperature and Forward Bias

The analyses from the temperature and forward bias step-stress testing show an altogether different degradation response than reverse bias stressing. For the reverse bias stressing, the population response was uniform, while the forward bias stressing population response was multi-modal. Some diodes did not degrade at all while other diodes from the same diffusion lot degraded progressively with temperature and current to catastrophic levels. The degradation response to forward current testing is much more dependent on V_M, the measurement bias voltage, than the reverse bias response. Thus, analyses of the results from such stressing involve attribute type analysis as well as intensive voltage-current characteristic studies prior to and after stress. Attribute analysis results should make it possible to estimate with confidence, the percentages of the different response classes in a random population. Further analysis would then be required to estimate the degradation rate of a given class of diodes as a function of the stress variables, T_S (temperature) and I_S (forward current).

The median reverse leakage current movement after each temperature step-stress readout (at fixed levels of forward current) is shown in Figure 41 for a measurement voltage of 15 volts. The movement at a measurement voltage of 30 volts is shown in Figure 42 and the movement for 50 volts is shown in Figure 43. The movement is shown for other percentiles, in chart form, in Figure 44 for a measurement voltage of 50 volts. The reverse leakage current response to forward current step-stress (at 100°C), is shown in Figure 45.

The abscissa is linear, reciprocal junction temperature. The junction temperature were calculated from the data obtained in the thermal resistance studies. Figure 46 is a graph which may be used to relate forward current, ambient temperature and the estimated junction temperature.

MEDIAN I_R vs. TEMPERATURE STEP STRESS WITH FIXED FORWARD CURRENT
(Stress Cells 12, 13, 14).

I_S = Forward Stress Current. V_M = Measurement Bias Voltage = 15 V.

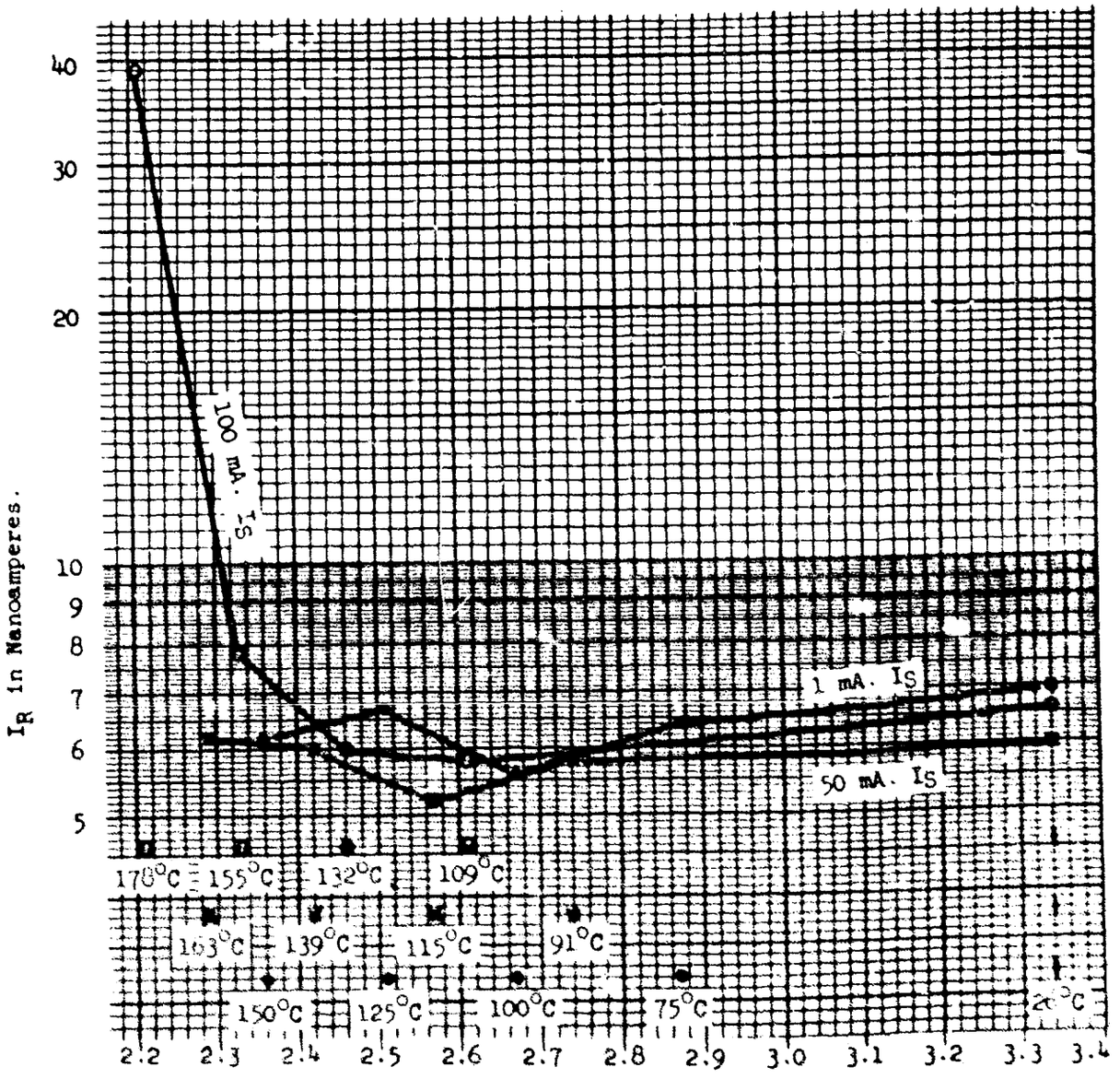


FIGURE 41

MEDIAN I_F vs. TEMPERATURE STEP STRESS WITH FIXED FORWARD CURRENT
(Stress Cells 12, 13, 14).

I_S = Forward Stress Current. V_M = Measurement Bias Voltage = 30 V.

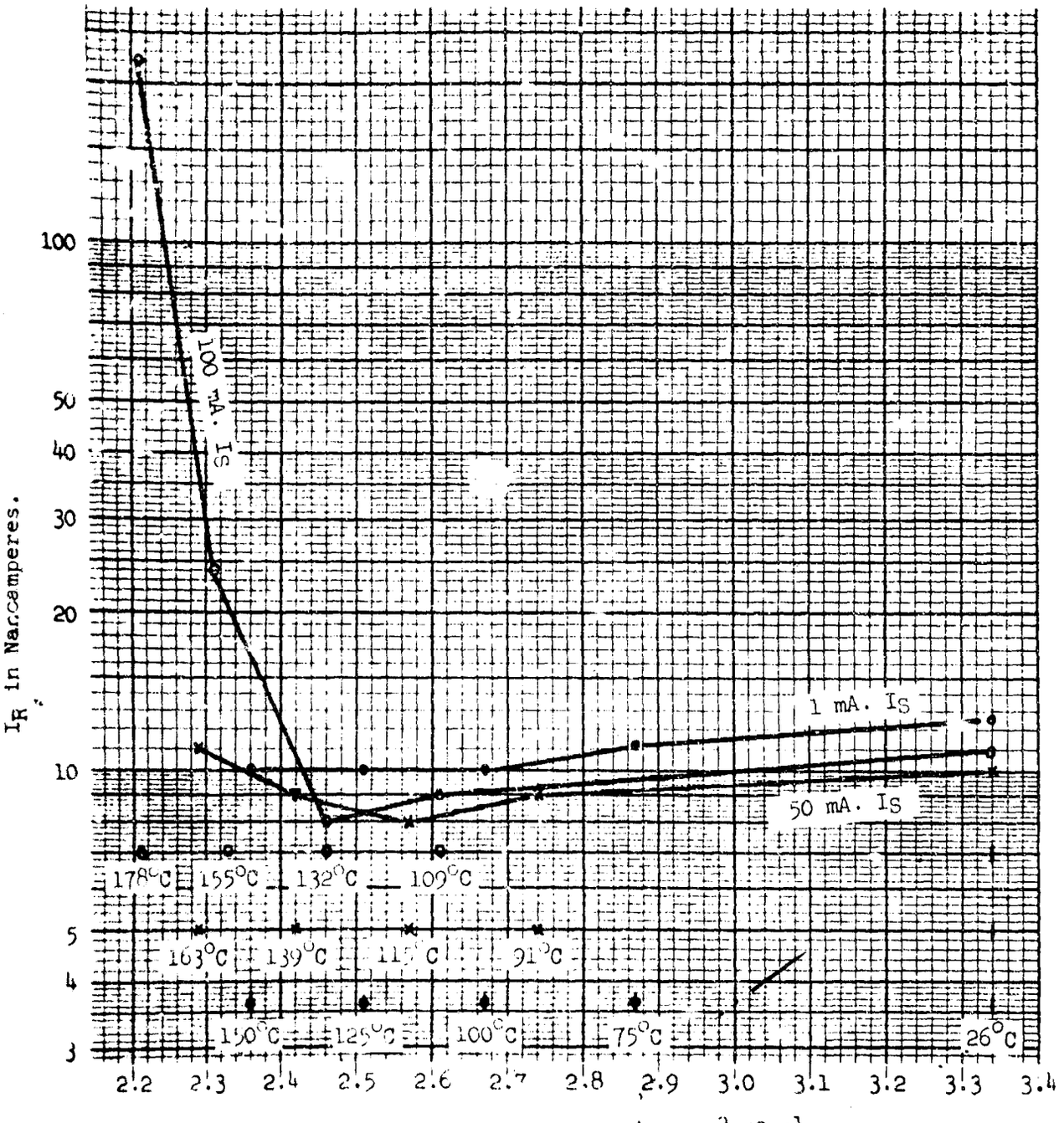


FIGURE 42

MEDIAN I_R vs. TEMPERATURE STEP STRESS WITH FIXED FORWARD CURRENT (Stress Cells 12, 13, 14).

I_S = Forward Stress Current. V_M = Measurement Bias Voltage = 50 V.

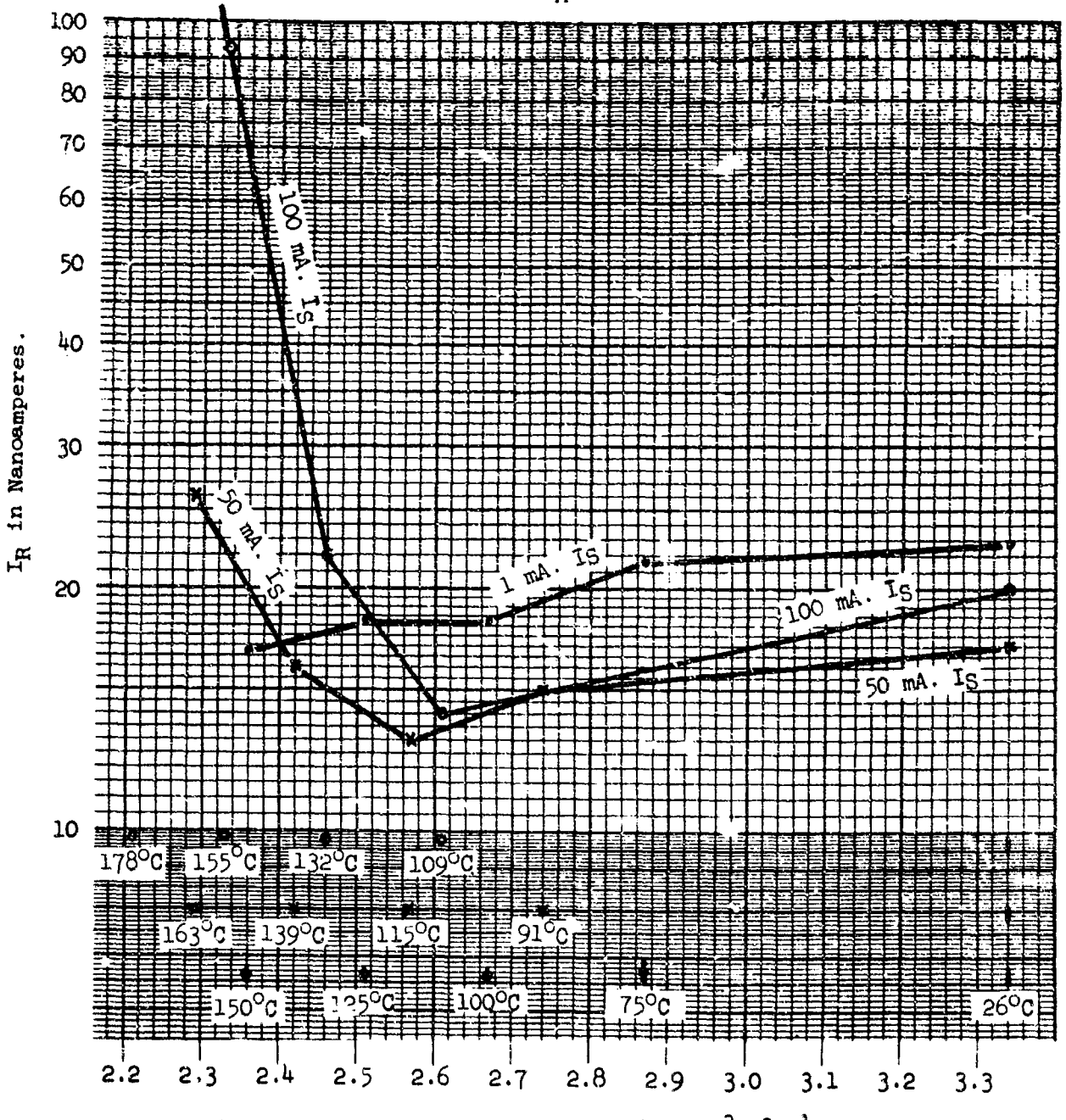


FIGURE 43

I_R @ V_M = 50 V. DEGRADATION UNDER ACCELERATED FORWARD CURRENT TESTING.

STRESS CELL 12 FIXED I_F = 1 mA.	INITIAL VALUES IN nA.	ESTIMATED MEAN JUNCTION TEMPERATURES 75°C.	100°C.	125°C.	150°C.
10th Percentile	12	1.0 X	0.9 X	0.9 X	0.7 X
25th Percentile	16	0.9 X	0.8 X	0.8 X	0.7 X
50th Percentile	23	0.9 X	0.8 X	0.8 X	0.7 X
75th Percentile	40	0.8 X	0.7 X	0.7 X	0.7 X
90th Percentile	46	0.9 X	0.8 X	0.9 X	1.0 X

STRESS CELL 13 FIXED I_F = 50 mA.	INITIAL VALUES IN nA.	ESTIMATED MEAN JUNCTION TEMPERATURES 70°C.	115°C.	159 °C.	164 °C.
10th Percentile	10	0.9 X	0.8 X	0.8 X	0.8 X
25th Percentile	14	0.9 X	0.8 X	0.8 X	0.7 X
50th Percentile	17	0.9 X	0.8 X	1.0 X	1.5 X
75th Percentile	22	1.0 X	1.2 X	1.5 X	14.1 X
90th Percentile	28	1.3 X	2.4 X	3.6 X	>

STRESS CELL 14 FIXED I_F = 100 mA.	INITIAL VALUES IN nA.	ESTIMATED MEAN JUNCTION TEMPERATURES 110°C	154°C	158°C	182°C
10th Percentile	10	0.8 X	0.8 X	1.3 X	3.6 X
25th Percentile	14	0.8 X	0.8 X	1.8 X	3.3 X
50th Percentile	20	0.7 X	1.1 X	4.7 X	27.0 X
75th Percentile	23	1.1 X	10.9 X	>	>
90th Percentile	40	1.9 X	68.8 X	>	>

STRESS CELL 11 FIXED T_A = 100°C.	INITIAL VALUES IN nA.	ESTIMATED MEAN JUNCTION TEMPERATURES 100°C. I_F=1 mA.	107°C. 25 mA.	115°C. 50 mA.	134°C. 100 mA	144°C. 125 mA	156°C. 150 mA
10th Percentile	10	0.8 X	0.9 X	1.0 X	1.0 X	1.0 X	1.0 X
25th Percentile	14	0.8 X	1.0 X	1.0 X	1.0 X	1.0 X	1.0 X
50th Percentile	19	0.9 X	1.1 X	1.1 X	1.1 X	2.2 X	2.4 X
75th Percentile	33	0.9 X	1.1 X	1.1 X	2.6 X	13.6 X	16.7 X
90th Percentile	42	0.9 X	1.1 X	1.4 X	11.1 X	72.1 X	>

Units removed for rejection (Assume greater than previous percentile).

FIGURE 44

PERCENTILES OF I_R vs. JUNCTION TEMPERATURE ON FORWARD CURRENT STEP STRESS AT FIXED AMBIENT TEMPERATURE (100°C.). (Stress Cell 11).

I_S = Forward Stress Current in mA. V_M = Measurement Bias Voltage = 50 V.
T_j = Junction Temperature in degrees Centigrade.

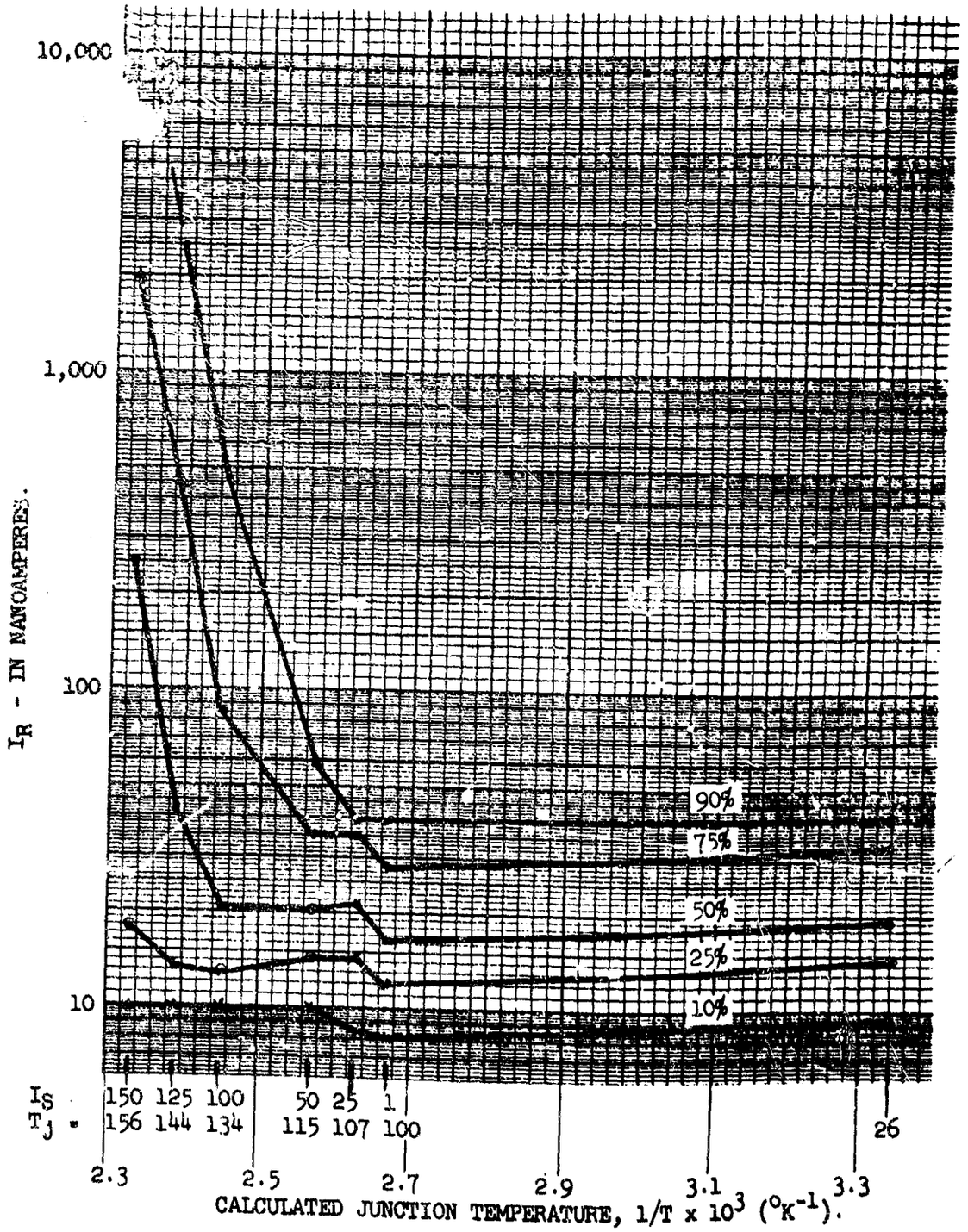


FIGURE 45

EXPECTED JUNCTION TEMPERATURES vs. OPERATING FORWARD CURRENT TESTS AT INDICATED AMBIENT TEMPERATURES (T_A).

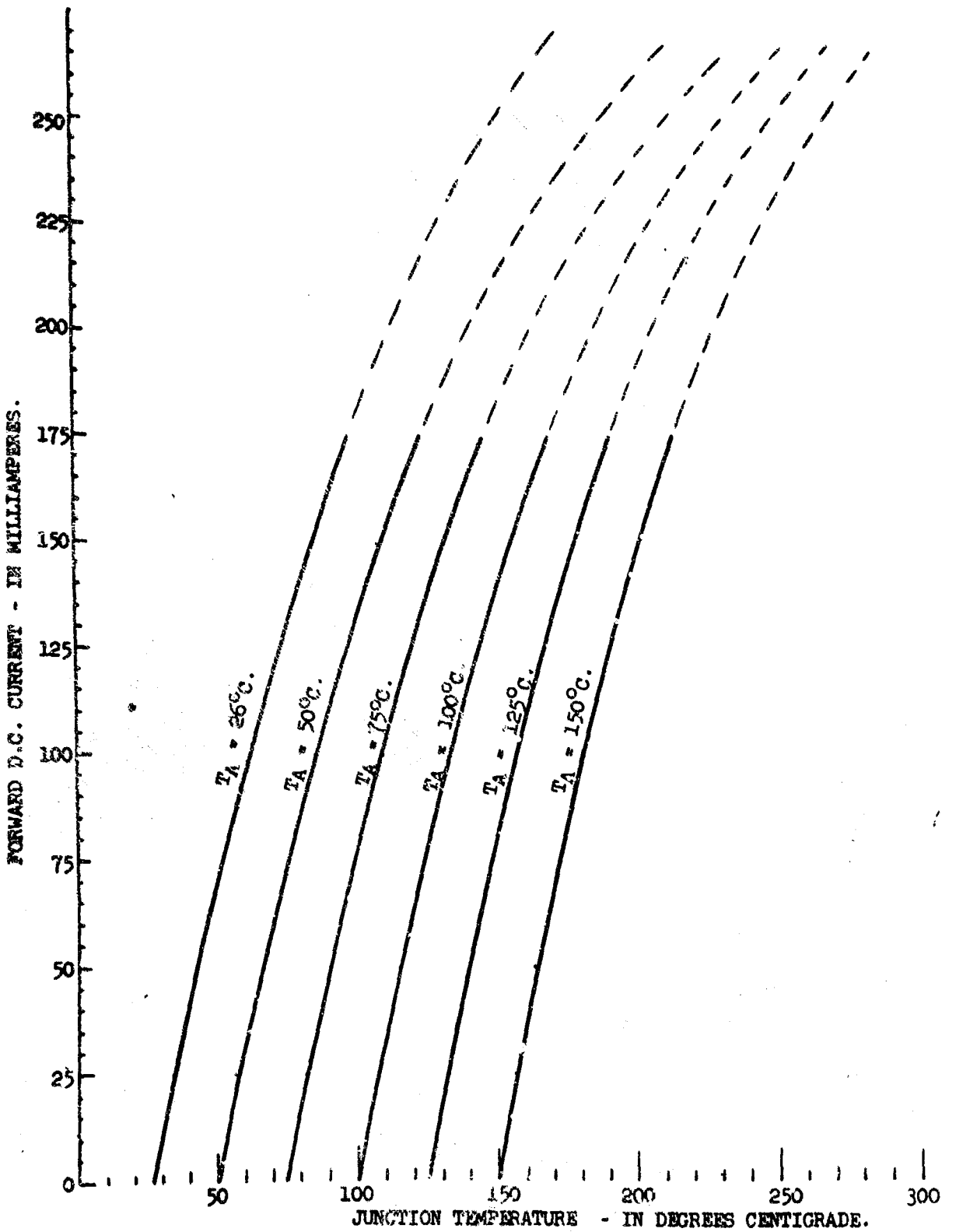


FIGURE 46

4.3 Long Term Constant Stress-in-Time

The parameter measurements have been made at the 9000 hour readout for the operating, temperature storage and temperature plus reverse bias long term tests. The 8000 hour measurements have been made for the forward bias long term test.

The observed reverse leakage current shift, as a function of time, is presented in four series of figures. Each series consists of six figures, one for each of the pellet diffusion lots. The entire distribution of the response is shown in each figure, for one of the original pellet diffusion lots. Thus, it is now possible to determine if there is any correlation between the degradation and a specific pellet lot. When test failures have been identified, and removed, this fact is noted on the appropriate figure. A table is inset in each figure which shows the pre-burn-in distribution of the reverse leakage current.

The response for the operating long term test (I_F = 450 mA peak, V_R = 30V peak) is shown in Figure 47-1 through 47-6. There has been very little response to this stress (as expected) except for one unit in diffusion lot 5. This unit was an A-2-a type failure, but it is not yet possible to assign any general failure response pattern to the population.

The temperature plus reverse bias long term test (T_A = 150°C, V_R = 30V) response is shown in Figure 48-1 through 48-6. There has been more response for this test than for the operating test, generally in the direction of an increase in the leakage current. Most of the failures that have been observed for this test have been determined to be non-legitimate, such as test equipment induced failures. The response pattern will continue to be observed,

to check for any possible degradation pattern.

The response for the temperature storage (T_A = 200°C) long term test is shown in Figure 49-1 through 49-6. Once again, the general response has been rather small (confirming the model), although several non-legitimate failures have been produced. A full discussion of these failures is contained in paragraph 2.3 of this report.

The forward bias (I_F = 50mA) long term test response is shown in Figure 50-1 through 50-6. There has been almost no response to this stress test which confirms the prediction of the model. The minimum value unit, for two of the diffusion lots, shifted downward but it is not yet possible to detect any general failure response pattern.

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 450 mA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 1

SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	10	-10
10%	12	- 8
25%	17	- 6
50%	23	- 2
75%	30	- 2
90%	38	+ 2
MAX	48	+24

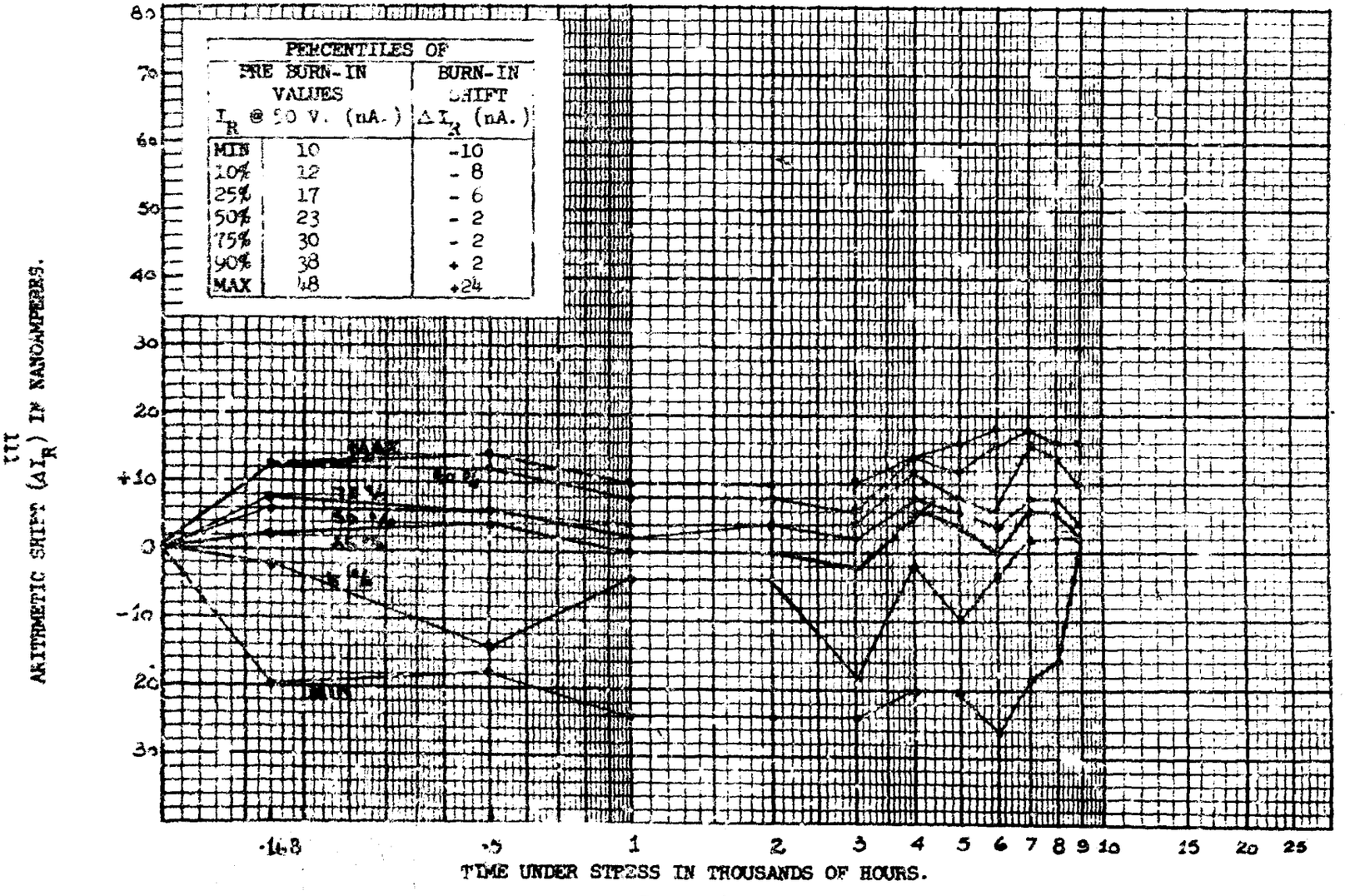


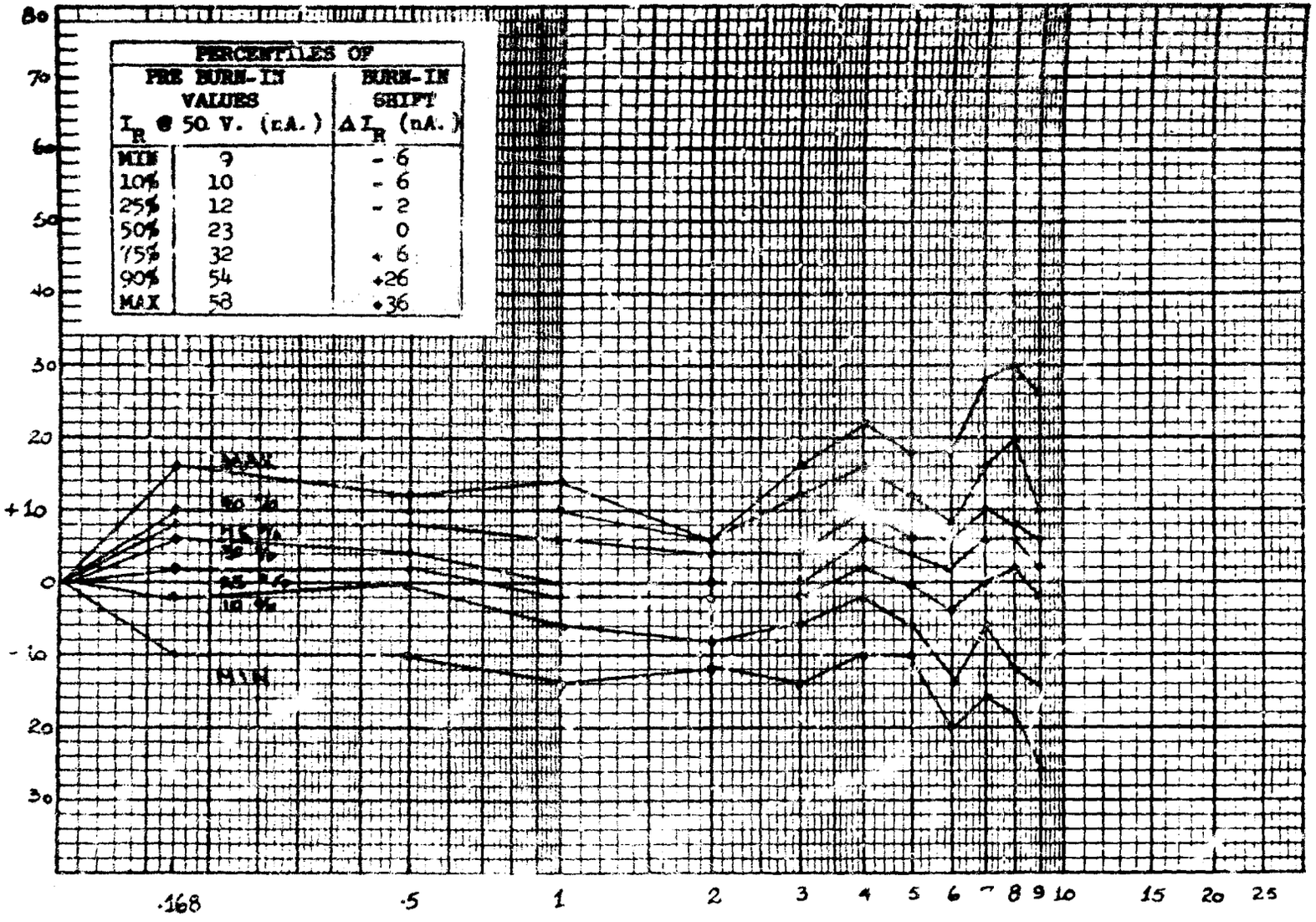
FIGURE 47-1

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 450 mA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 2

SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	9	- 6
10%	10	- 6
25%	12	- 2
50%	23	0
75%	32	+ 6
90%	54	+26
MAX	58	+36



ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 47-2

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 450 MA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 3

SAMPLE SIZE: 20

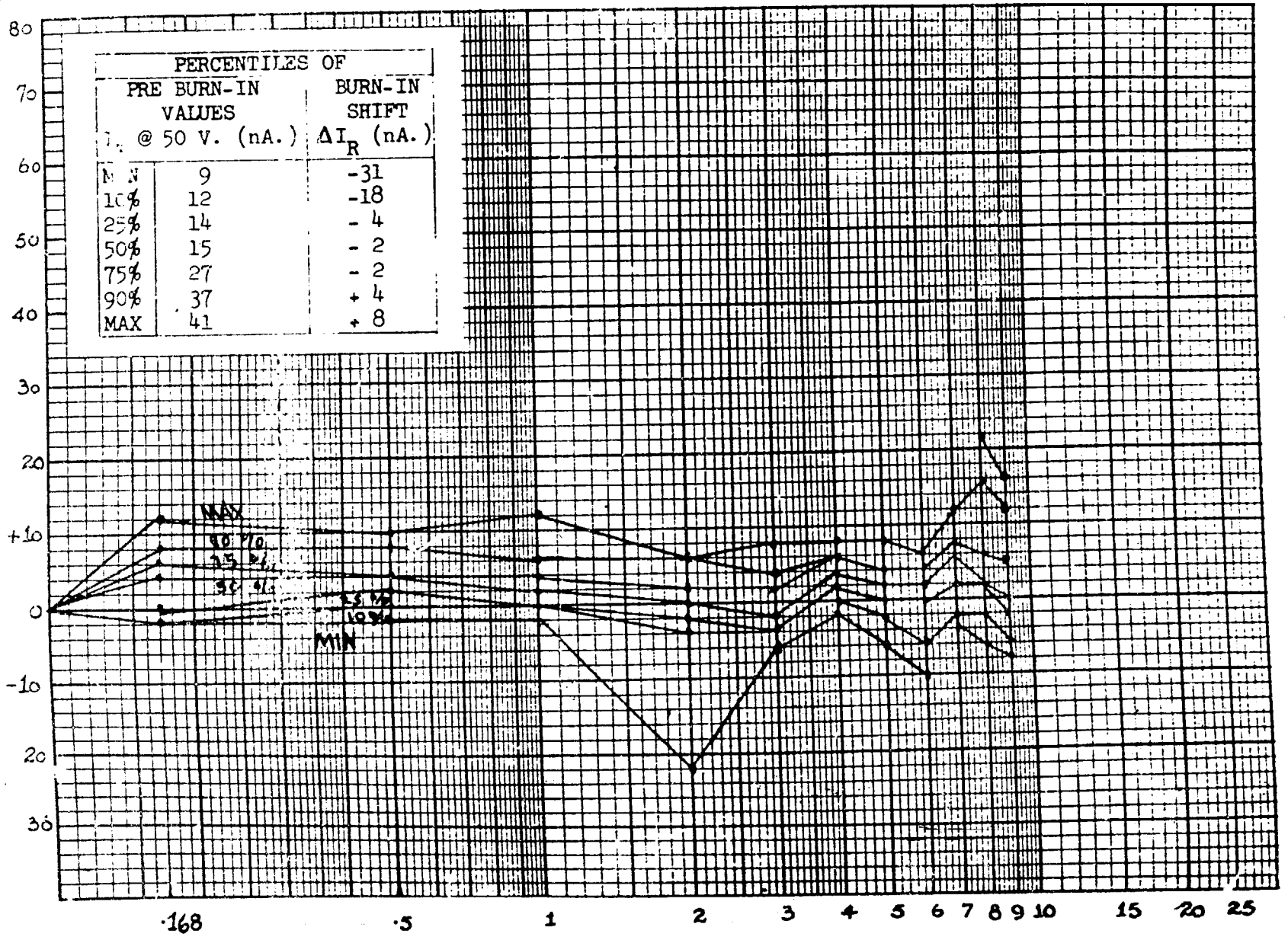


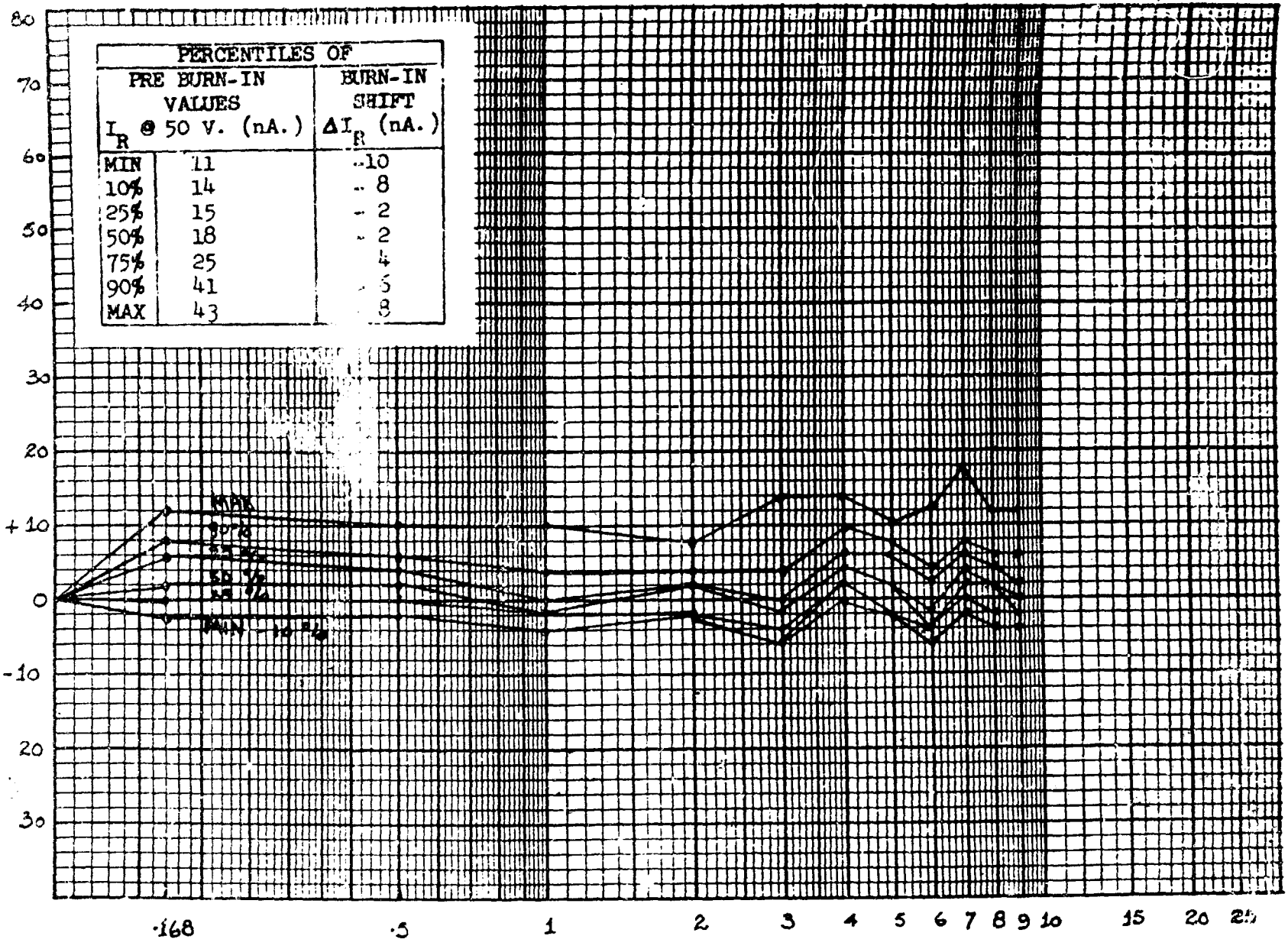
FIGURE 47-3

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 450 mA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 4

SAMPLE SIZE: 43

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	11	-10
10%	14	- 8
25%	15	- 2
50%	18	- 2
75%	25	4
90%	41	- 5
MAX	43	8



ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 47-4

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 40 mA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 5

SAMPLE SIZE: 20

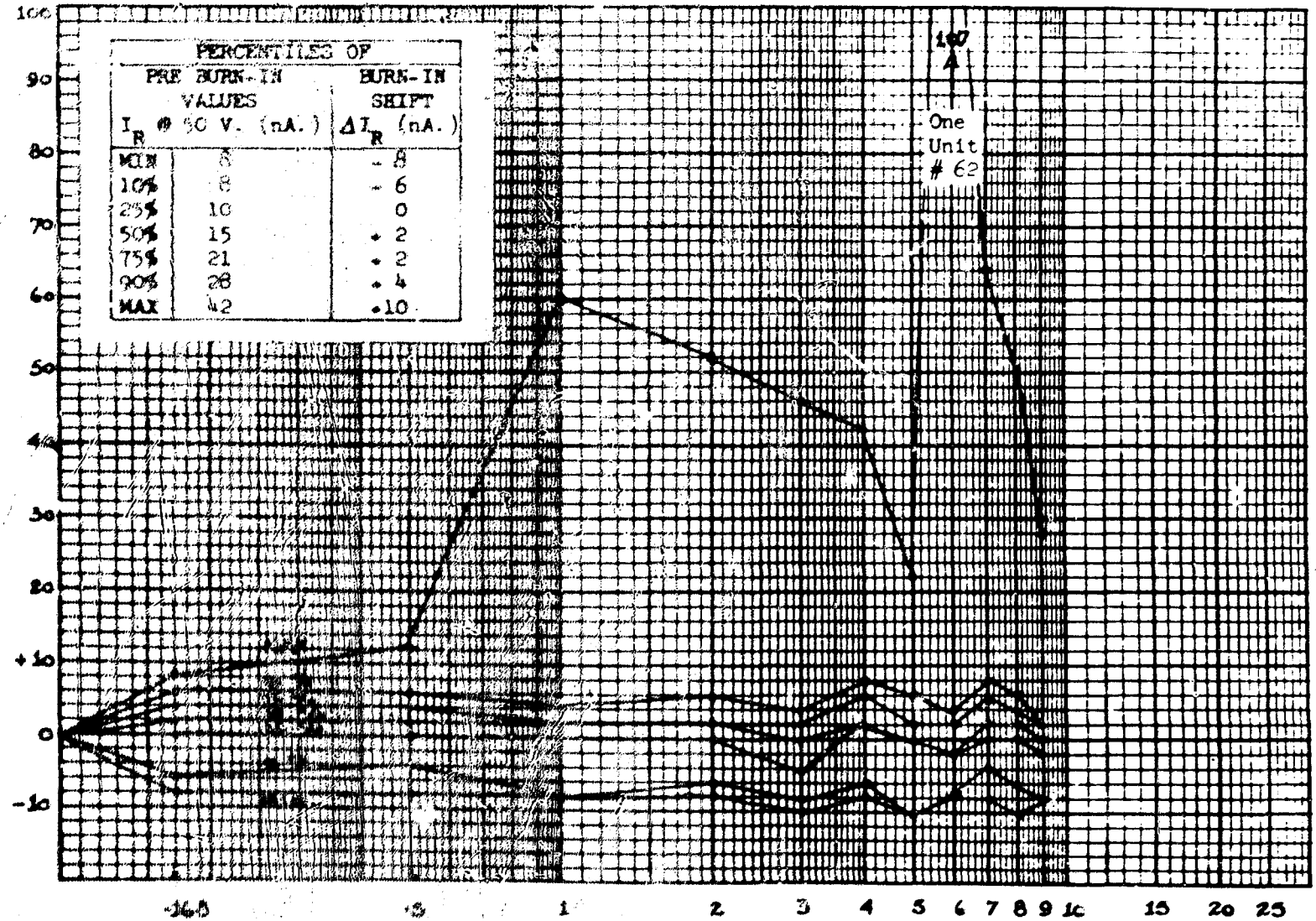


FIGURE 47-5

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL RECTIFYING OPERATING STRESS OF FORWARD 50 mA. (PEAK) AND REVERSE 30 V. (PEAK) AT ROOM TEMPERATURE. (STRESS CELL 1).

DIFFUSION LOT: 6

SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	13	- 2
10%	14	- 2
25%	16	+ 2
50%	18	+ 2
75%	20	+ 2
90%	21	+ 4
MAX	23	+ 6

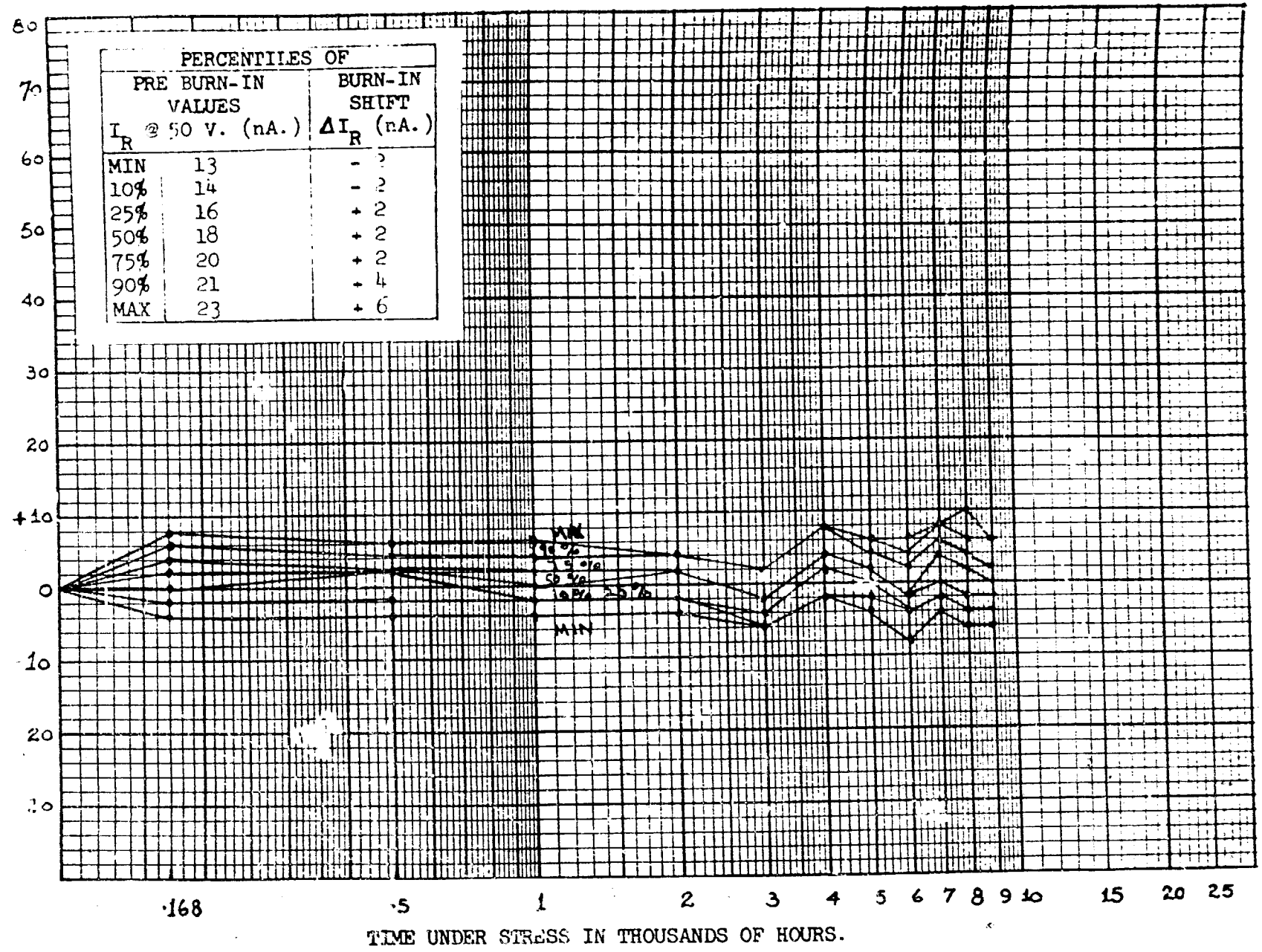


FIGURE 47-6

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) (STRESS CELL 2).

DIFFUSION LOT: 1
SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	14	-12
10%	15	-12
25%	18	- 6
50%	24	- 4
75%	30	- 2
90%	39	+ 2
MAX	42	+10

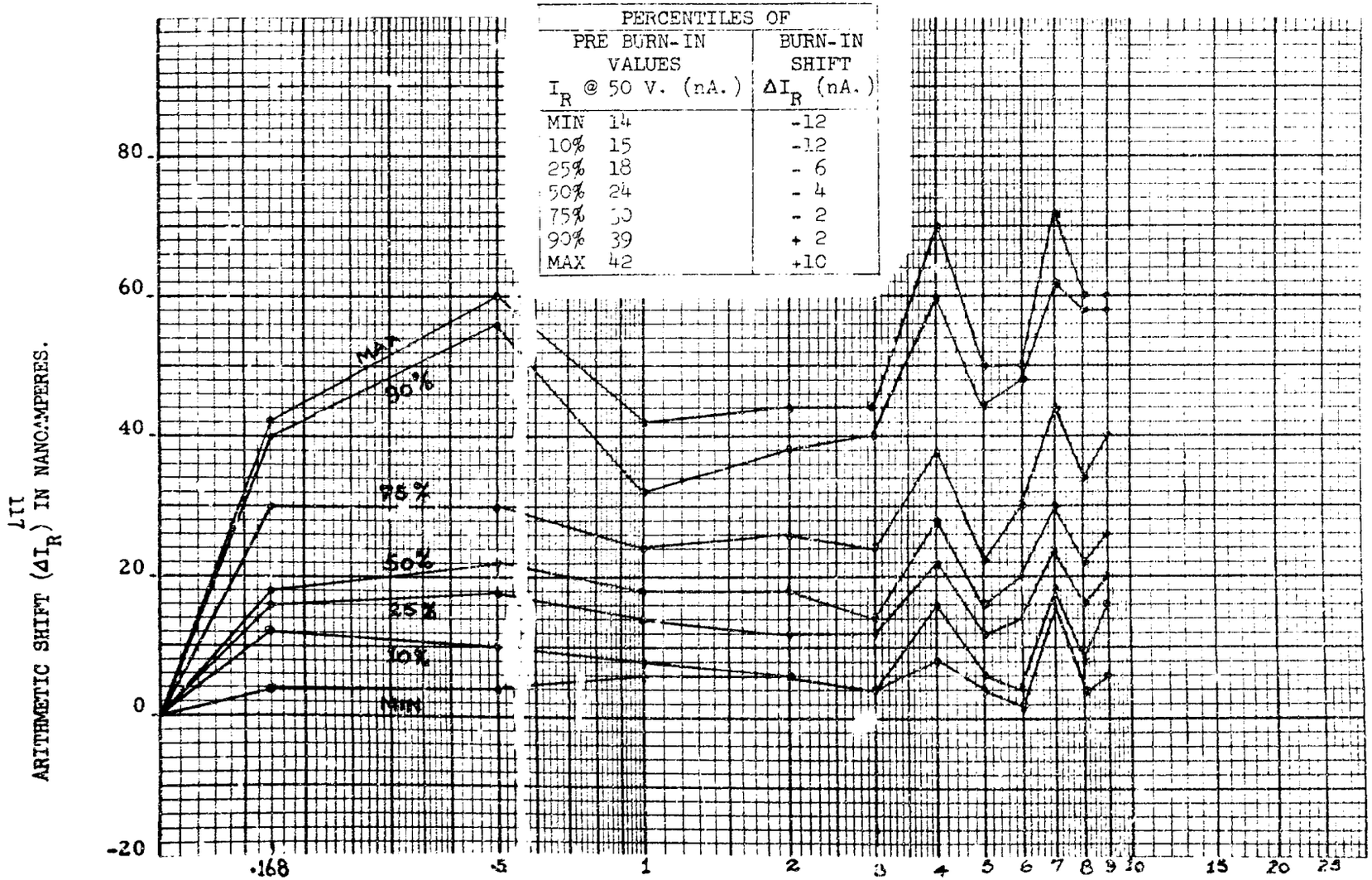


FIGURE 48-1

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) (STRESS CELL 2).

DIFFUSION LOT: 2
SAMPLE SIZE: 20

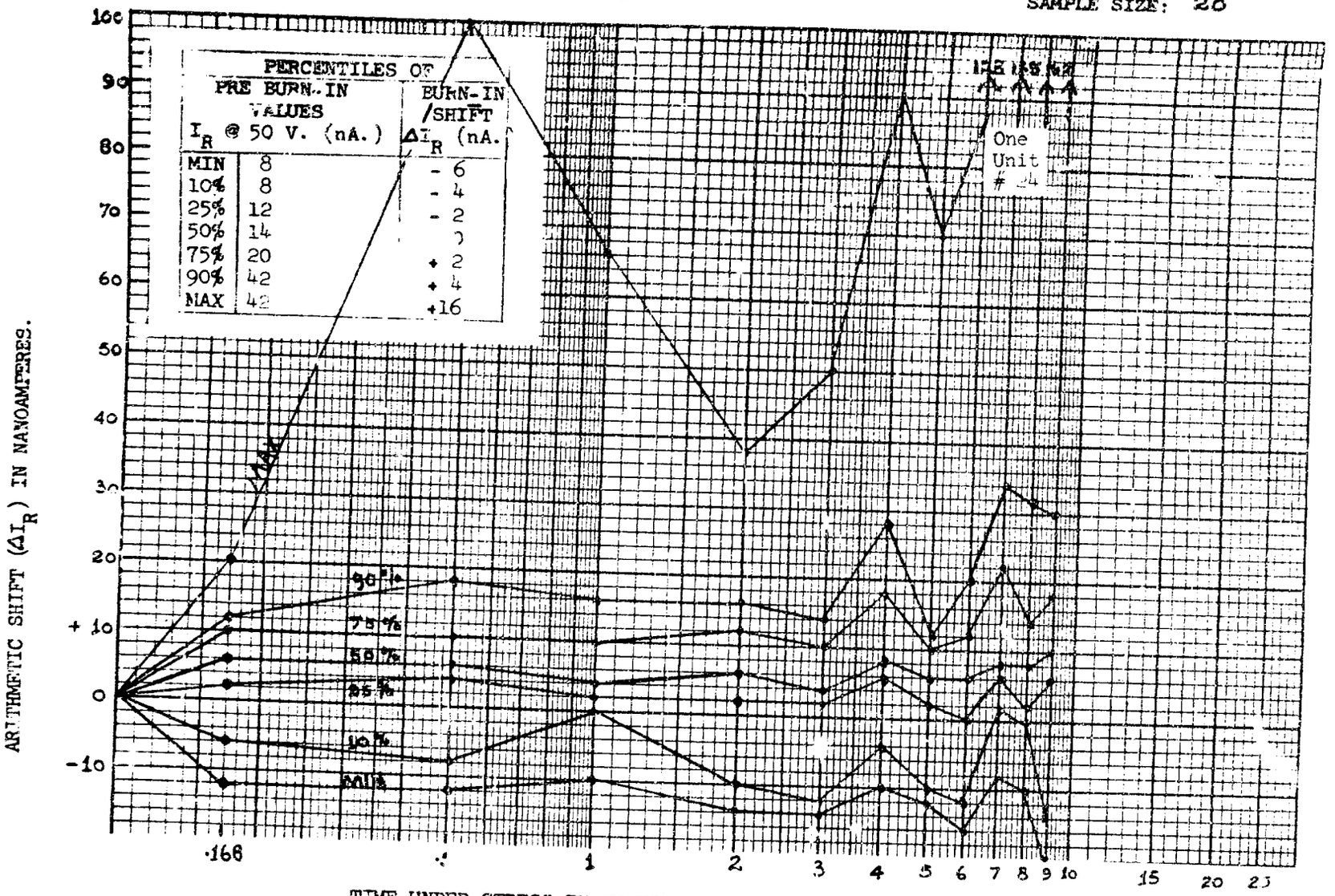


FIGURE 48-2

PERCENTILES OF ARITHMETIC SHIFT OF I_F @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) (STRESS CELL 2).

DIFFUSION LOT: 3
SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	10	-10
10%	12	- 8
25%	14	- 2
50%	17	- 2
75%	38	- 2
90%	42	+ 2
MAX	49	+ 4

* = Unit removed. Failure Analysis Report # 45. (Unit # 19).

ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 48-3

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) (STRESS CELL 2).

DIFFUSION LOT: 4
SAMPLE SIZE: 20

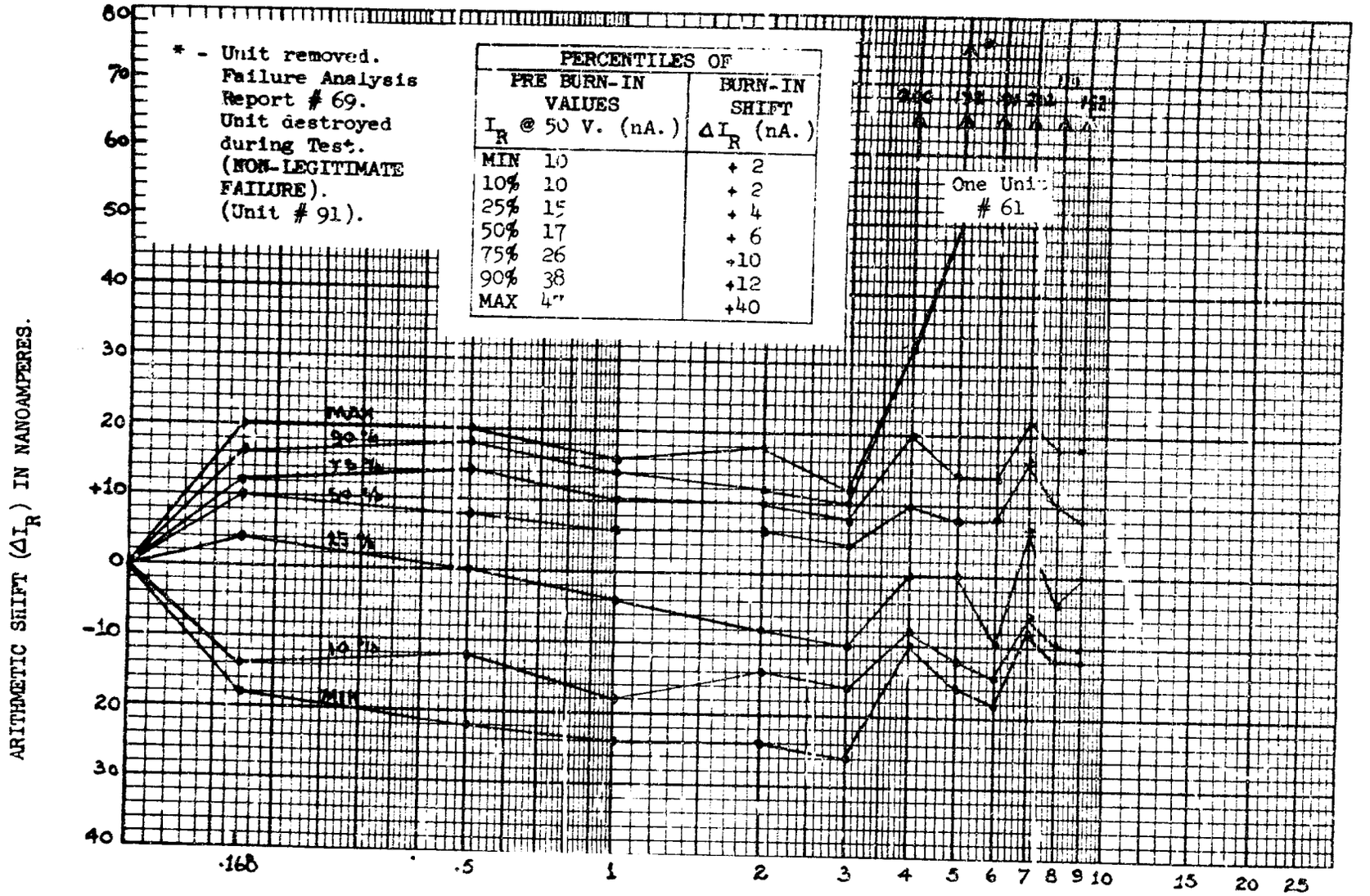
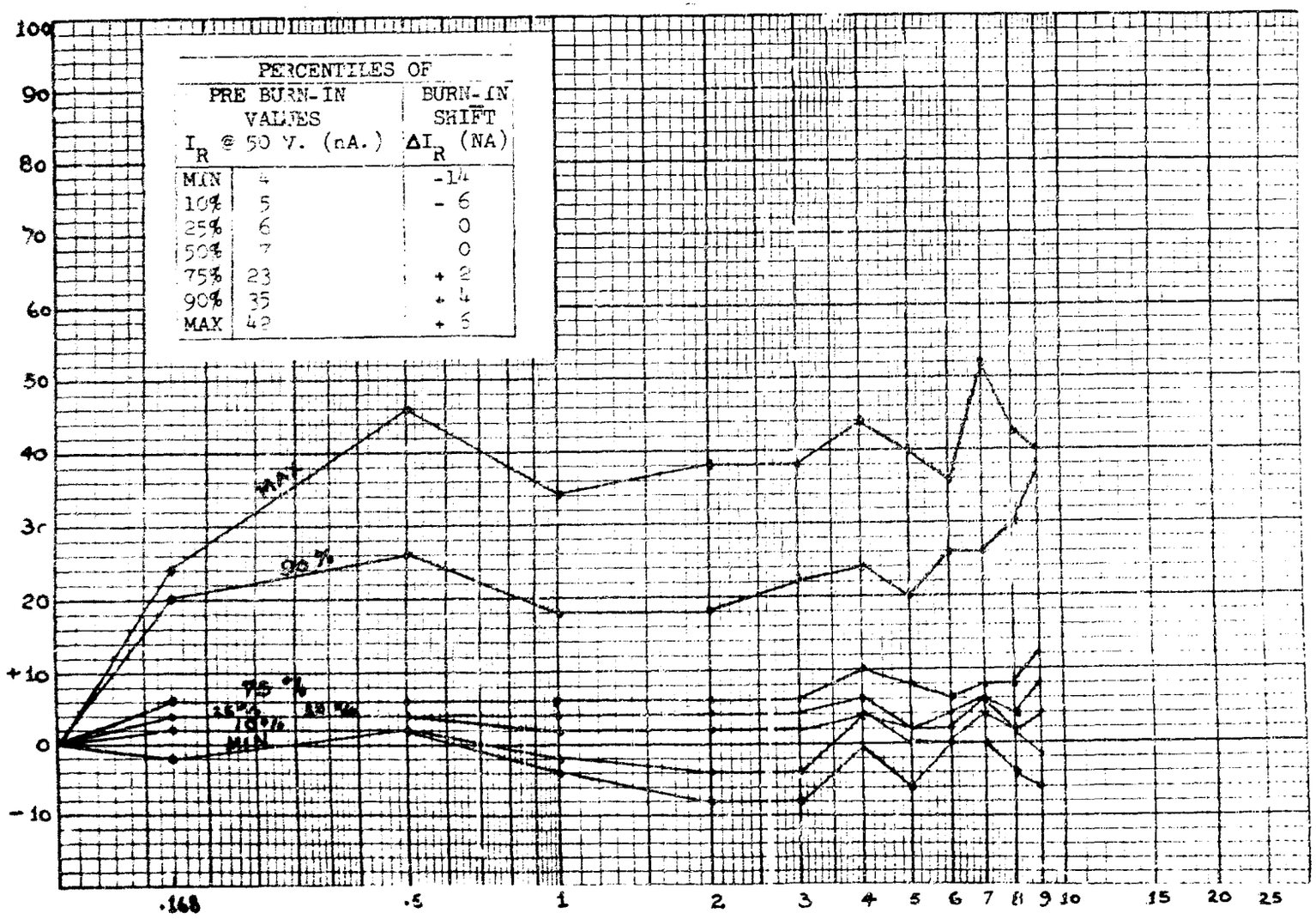


FIGURE 48-4

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) (STRESS CELL 2).

DIFFUSION LOT: 5
SAMPLE SIZE: 20

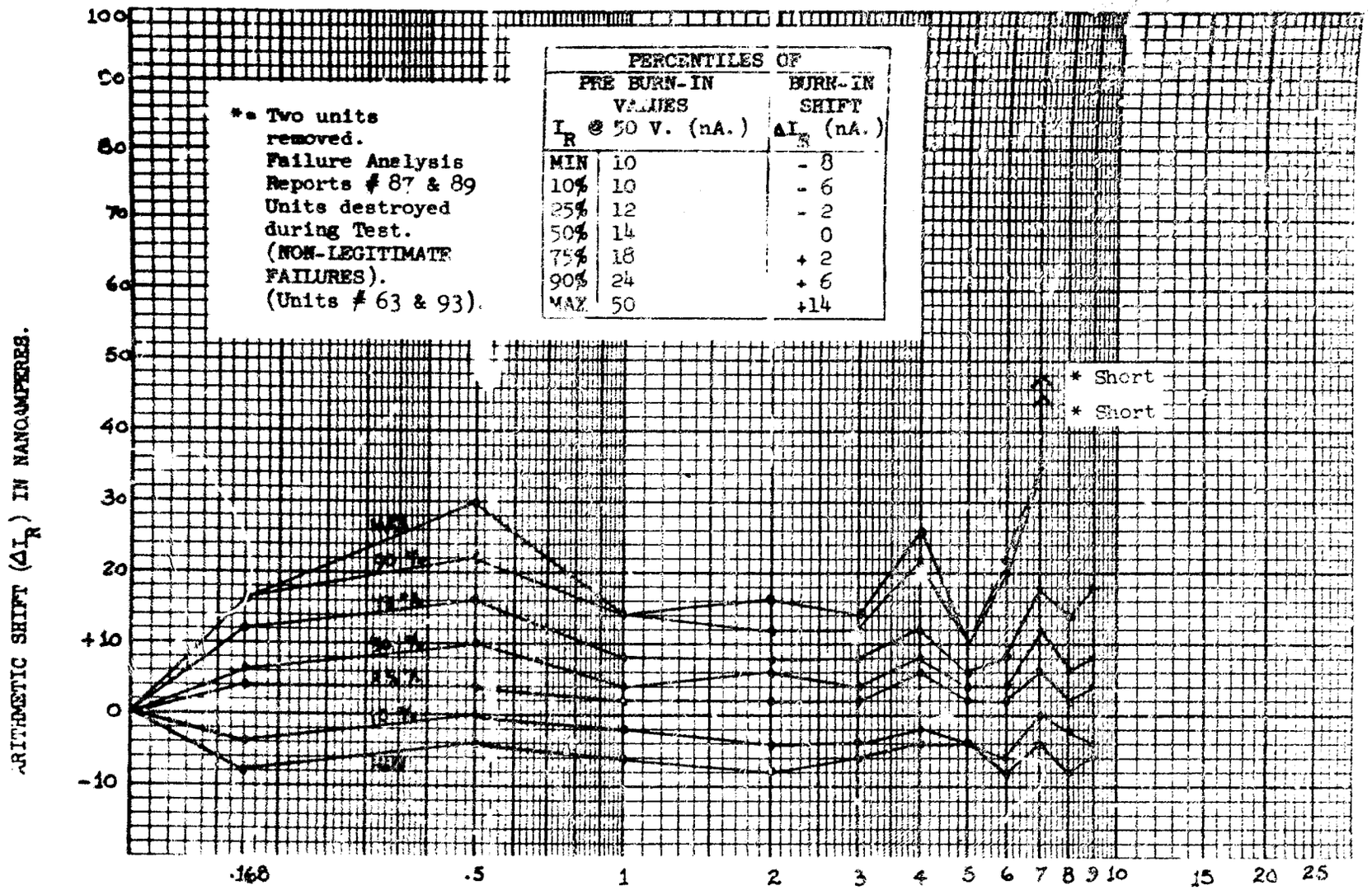


ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 68-5

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL STRESS OF TEMPERATURE (T_A = 150°C.) AND REVERSE VOLTAGE (V_S = 30 V.) STRESS CELL 2). DIFFUSION LOT: 6 SAMPLE SIZE: 20



PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	10	- 8
10%	10	- 6
25%	12	- 2
50%	14	0
75%	18	+ 2
90%	24	+ 6
MAX	50	+14

** Two units removed. Failure Analysis Reports # 87 & 89 Units destroyed during Test. (NON-LEGITIMATE FAILURES). (Units # 63 & 93).

FIGURE 48-6

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (200°C.). (STRESS CELL 3).

DIFFUSION LOT: 1
SAMPLE SIZE: 19

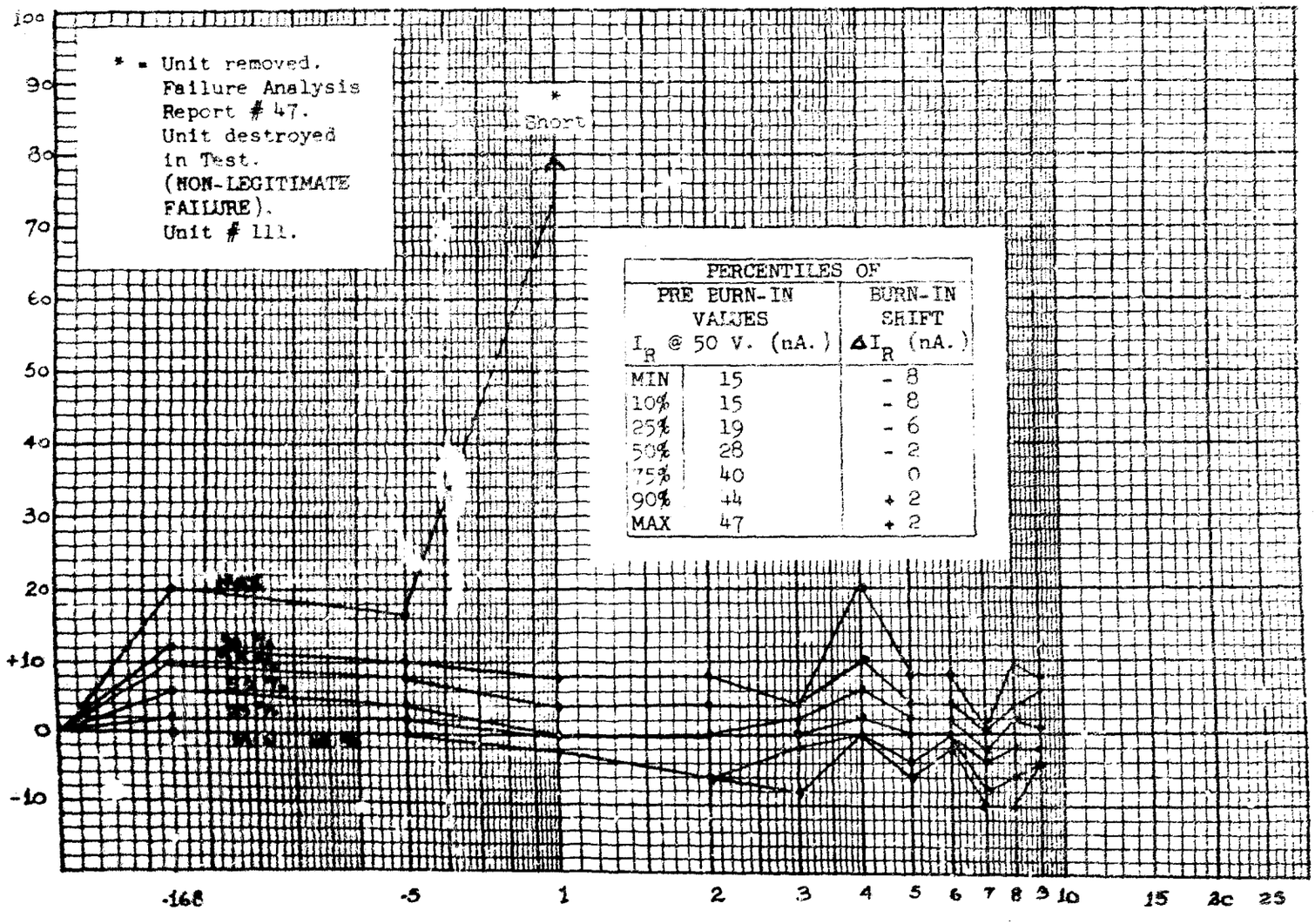


FIGURE 49-1

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (150°C.). (STRESS CELL 1).

DIFFUSION LOT: 2
SAMPLE SIZE: 21

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	8	- 4
[illegible]	8	- 2
[illegible]	12	- 2
[illegible]	14	0
[illegible]	19	0
[illegible]	25	+ 2
MAX	29	+ 2

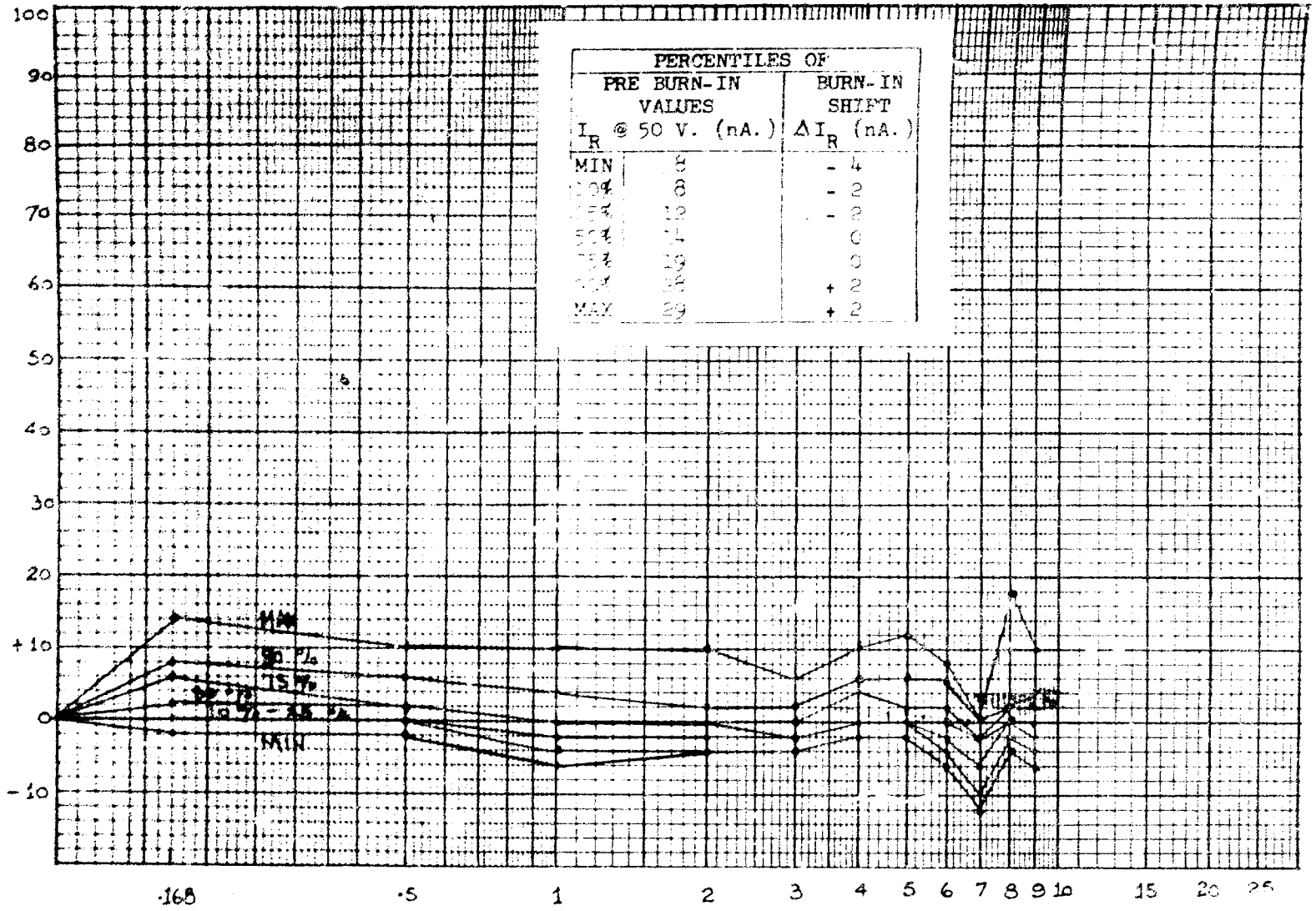


FIGURE 49-2

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (200°C.). (STRESS CELL 3).

DIFFUSION LOT: 3
SAMPLE SIZE: 20

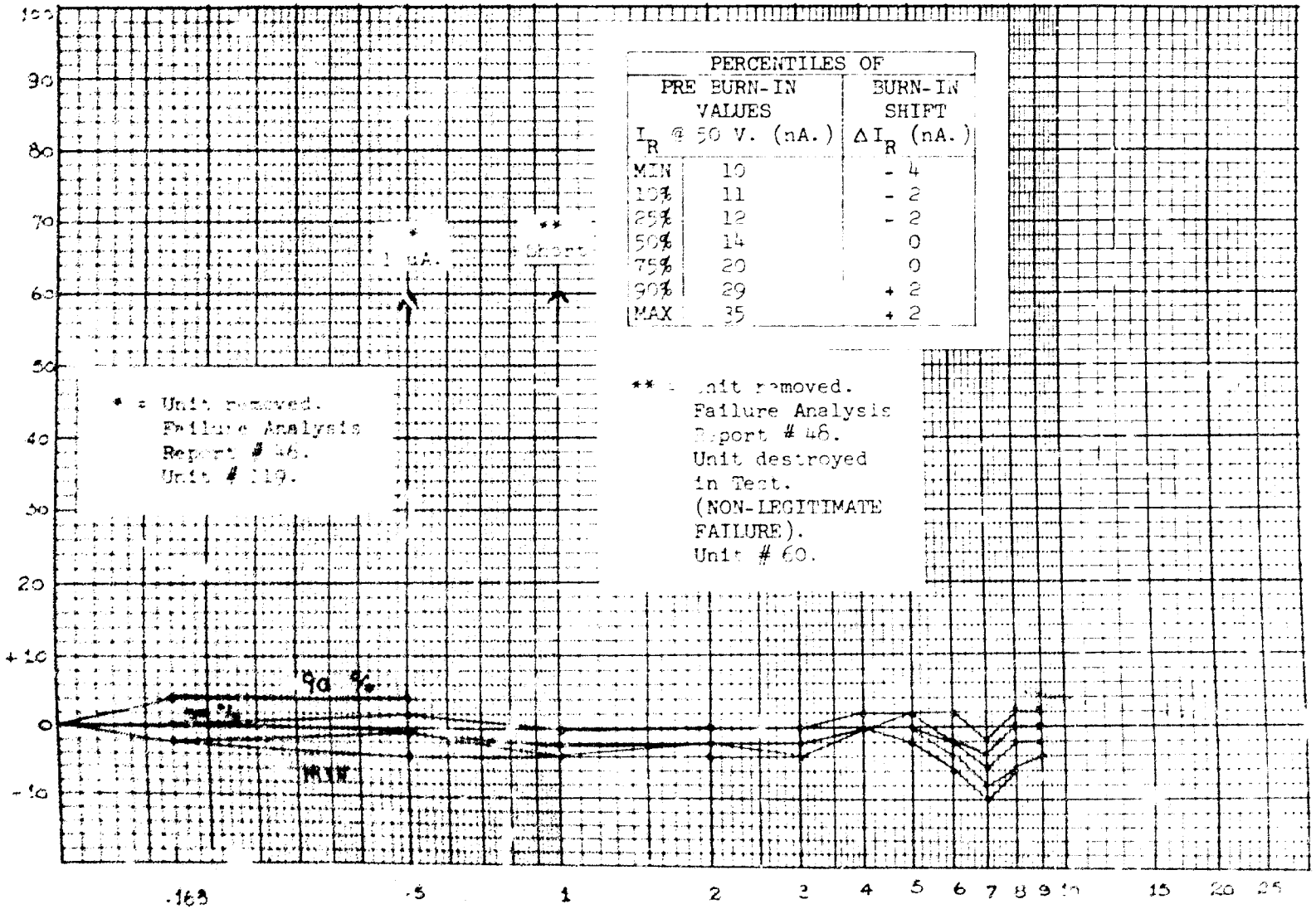


FIGURE 49-3

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (200°C.). (STRESS CELL 3).

DIFFUSION LOT: 4
SAMPLE SIZE: 21

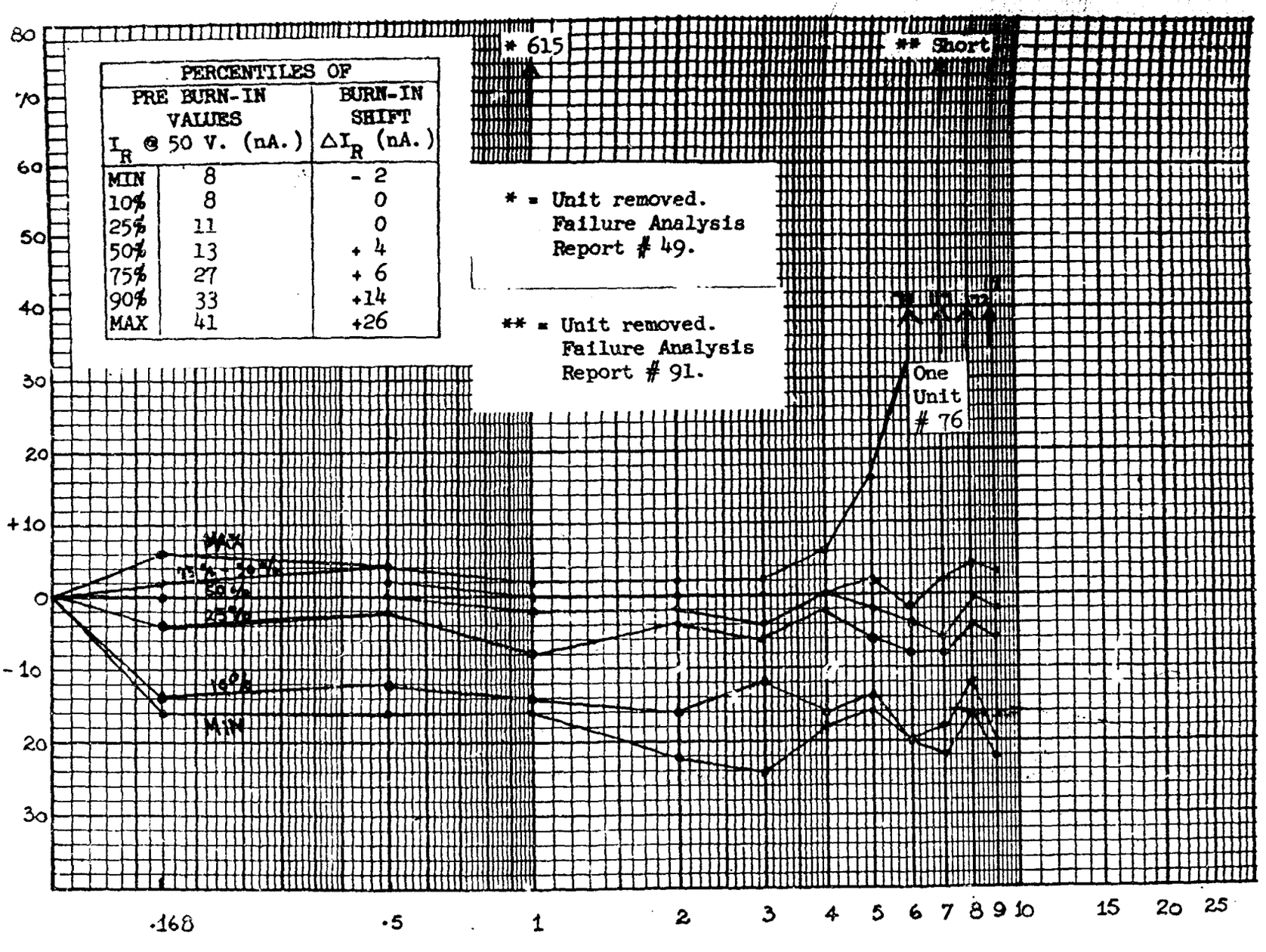


FIGURE 19-4

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (200°C.). (STRESS CELL 3).

DIFFUSION LOT: 5
SAMPLE SIZE: 18

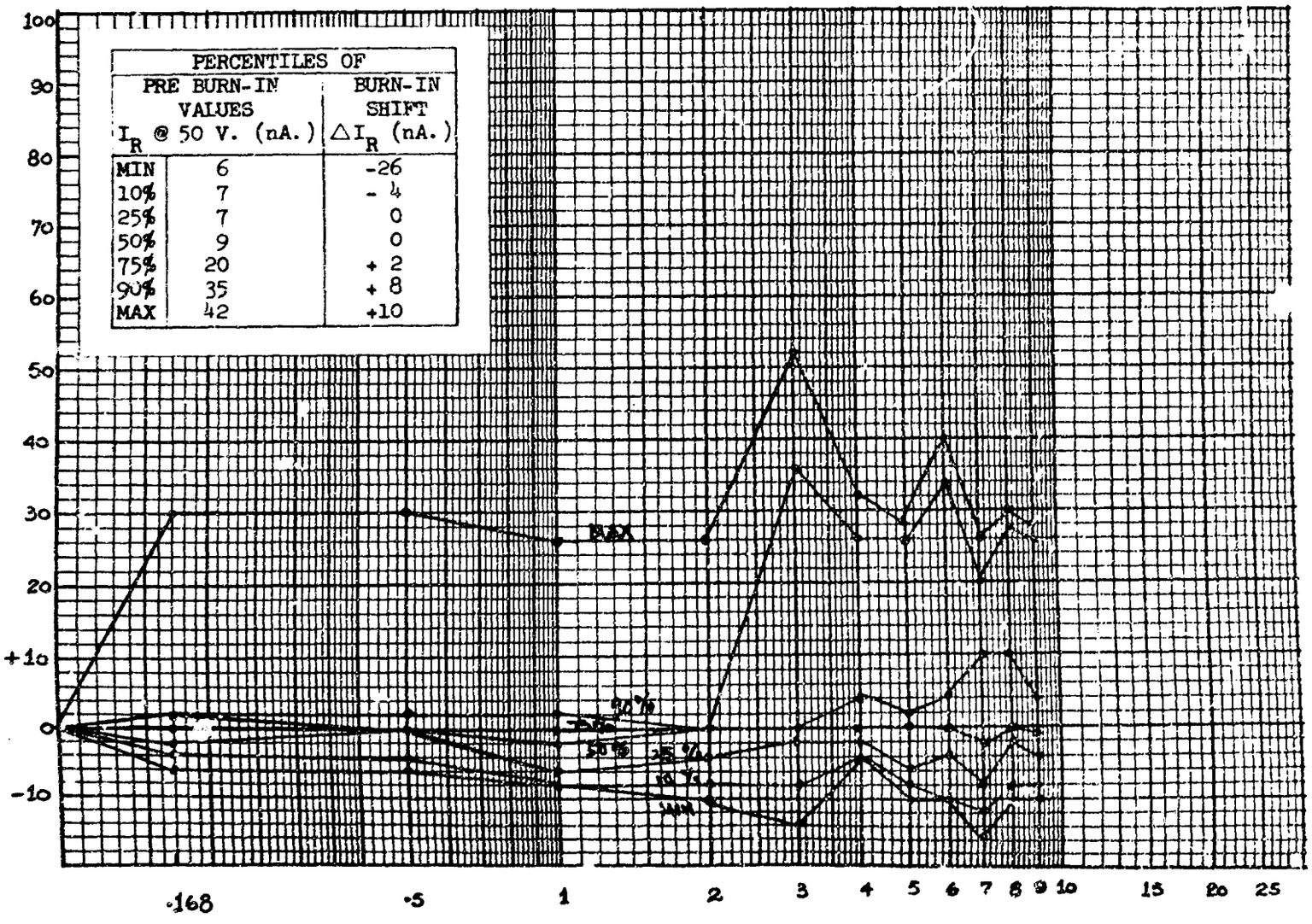
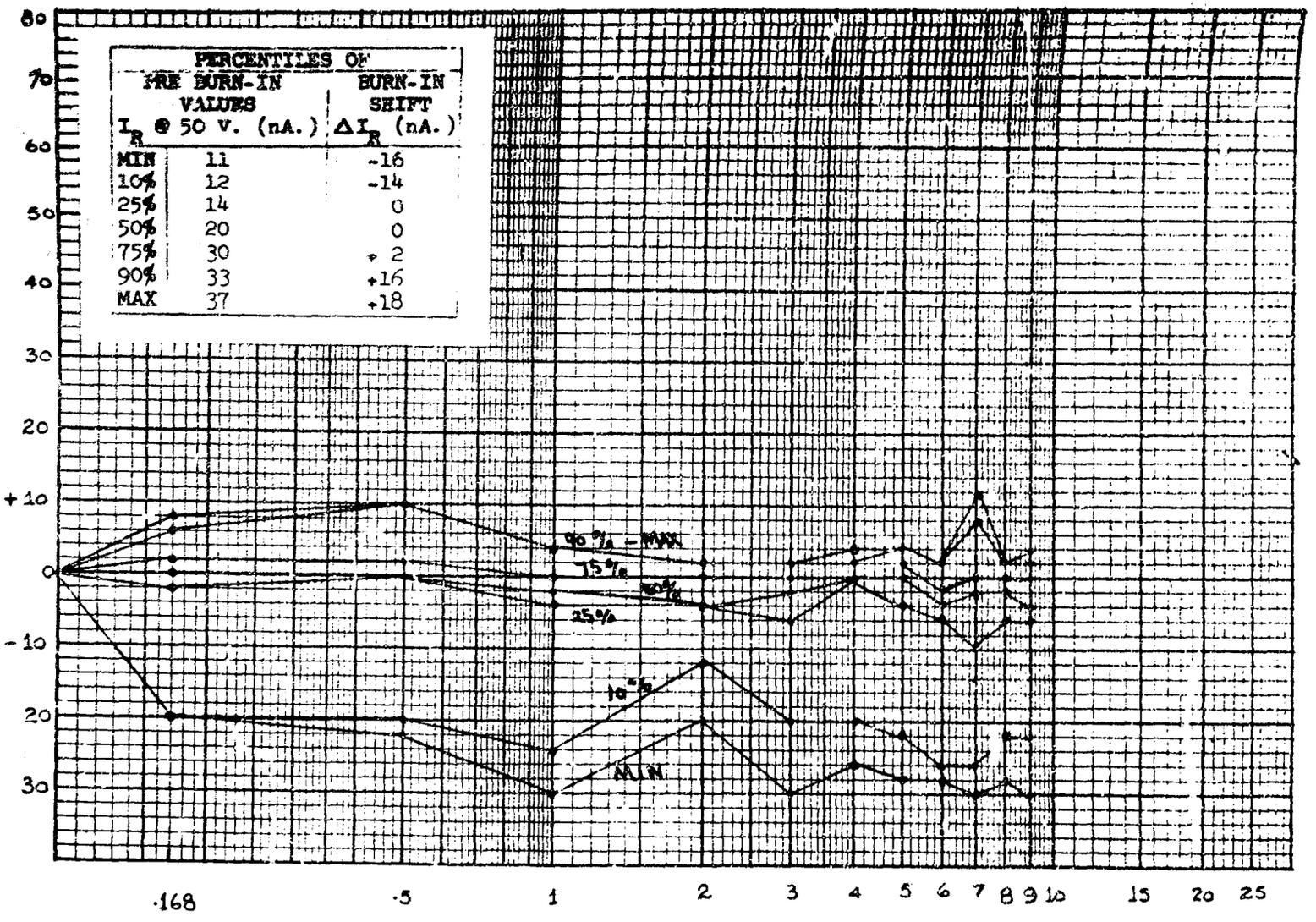


FIGURE 49-5

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUE FOR LONG TERM LOW LEVEL TEMPERATURE STORAGE (200°C.). (STRESS CELL 3).

DIFFUSION LOT: 6
SAMPLE SIZE: 17



ARITHMETIC SHIFT (I_R) IN NANOAMPERES.

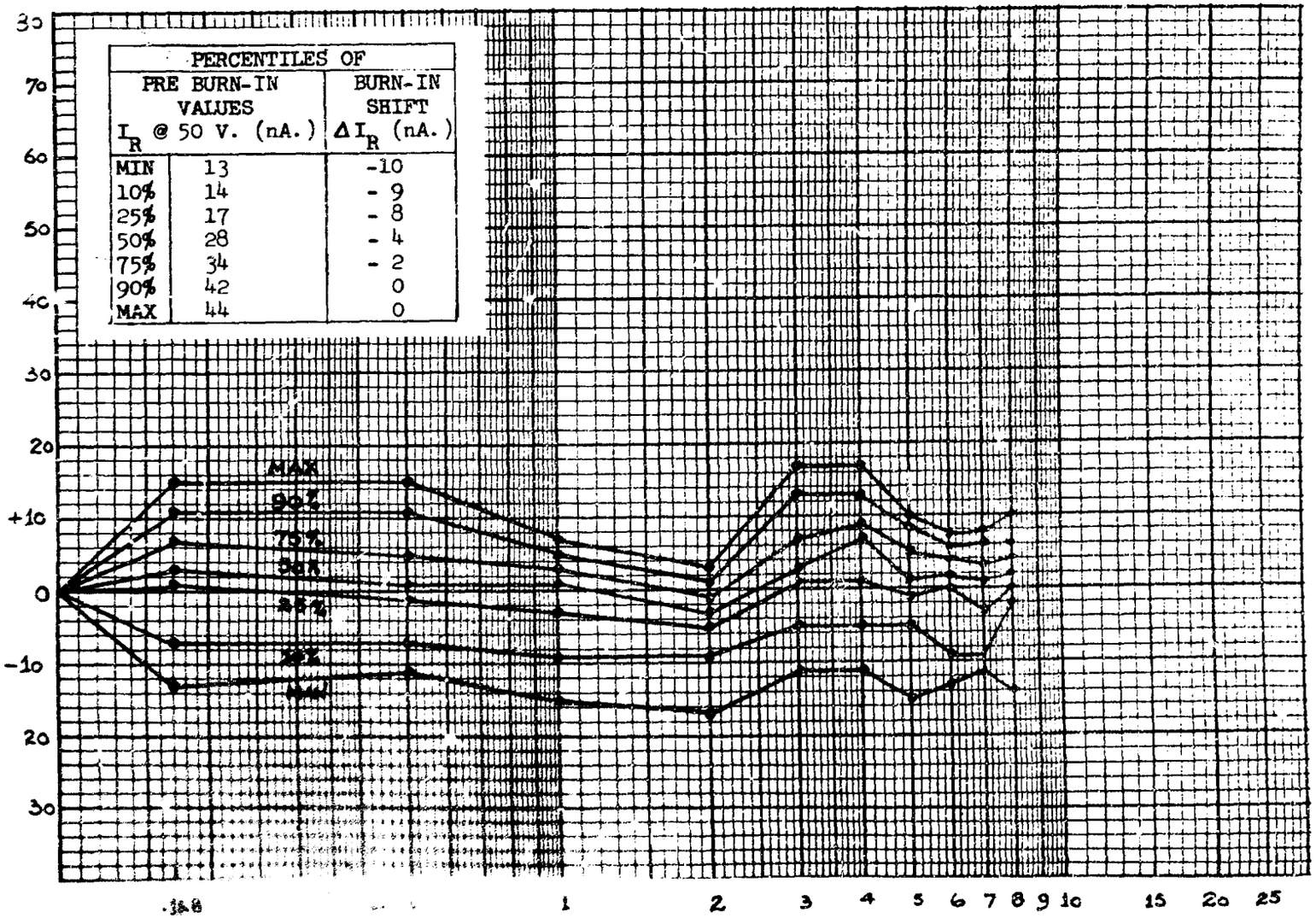
128

FIGURE 49-6

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 mA. AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: 1
SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	13	-10
10%	14	- 9
25%	17	- 8
50%	28	- 4
75%	34	- 2
90%	42	0
MAX	44	0



ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME IN HOURS IN THOUSANDS OF HOURS.

FIGURE 50-1

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 mA. AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: 2
SAMPLE SIZE: 20

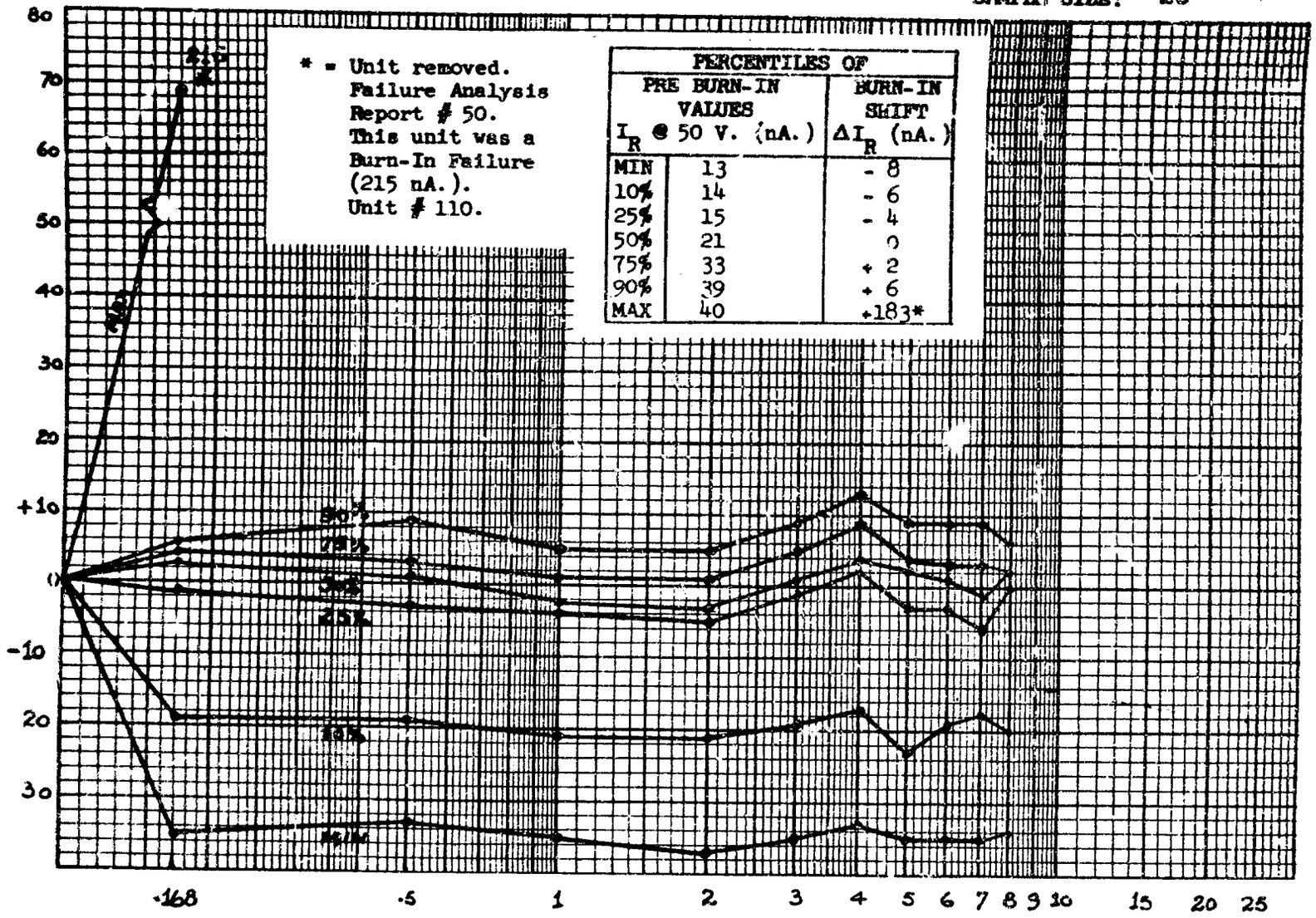
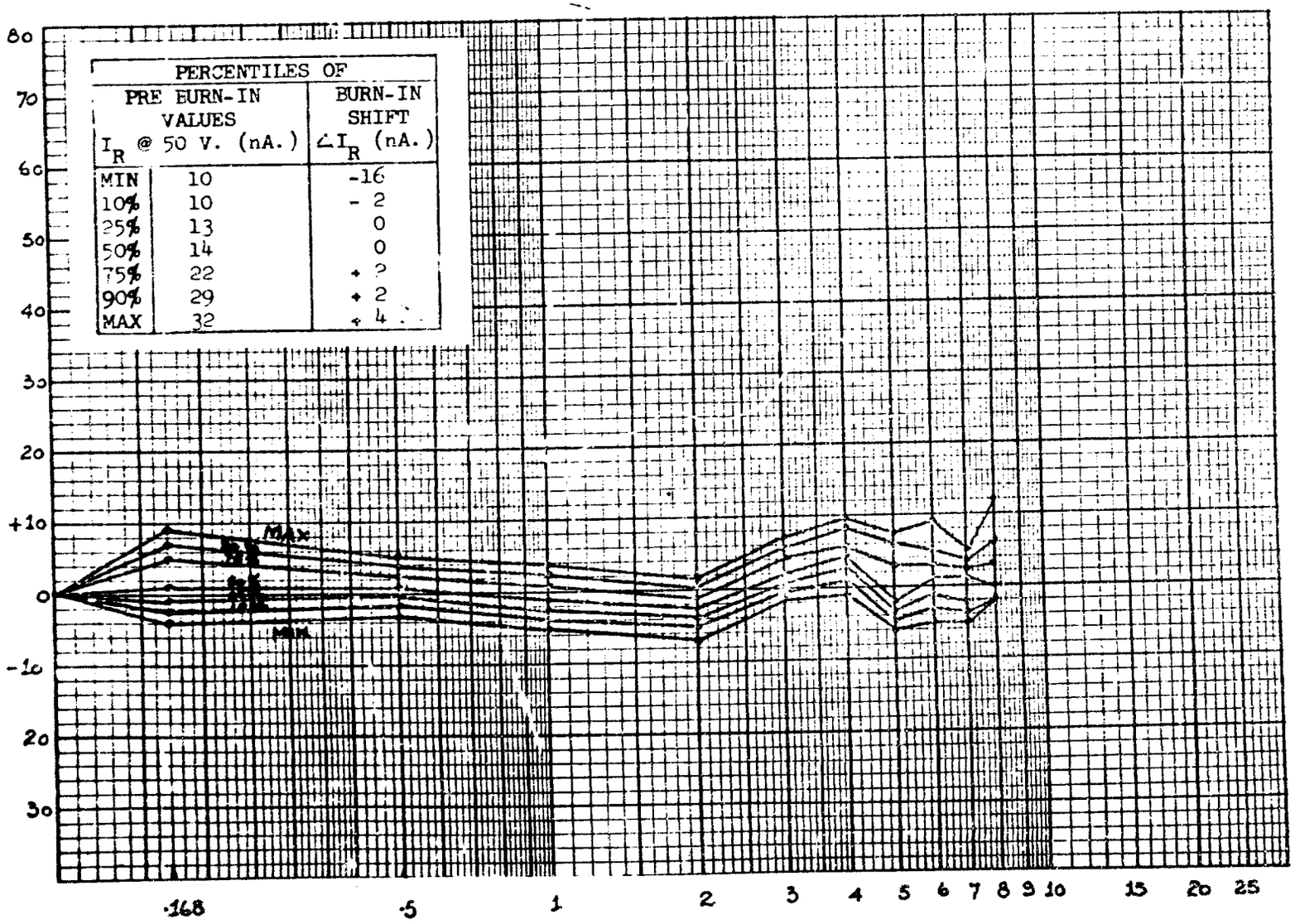


FIGURE 50-2

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 nA. AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: 3
SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	10	-16
10%	10	- 2
25%	13	0
50%	14	0
75%	22	+ 2
90%	29	+ 2
MAX	32	+ 4



ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 50-3

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 mA AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: 4
SAMPLE SIZE: 20

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	6	- 8
10%	8	- 4
25%	12	0
50%	17	+ 4
75%	27	+ 6
90%	44	+ 8
MAX	49	+10

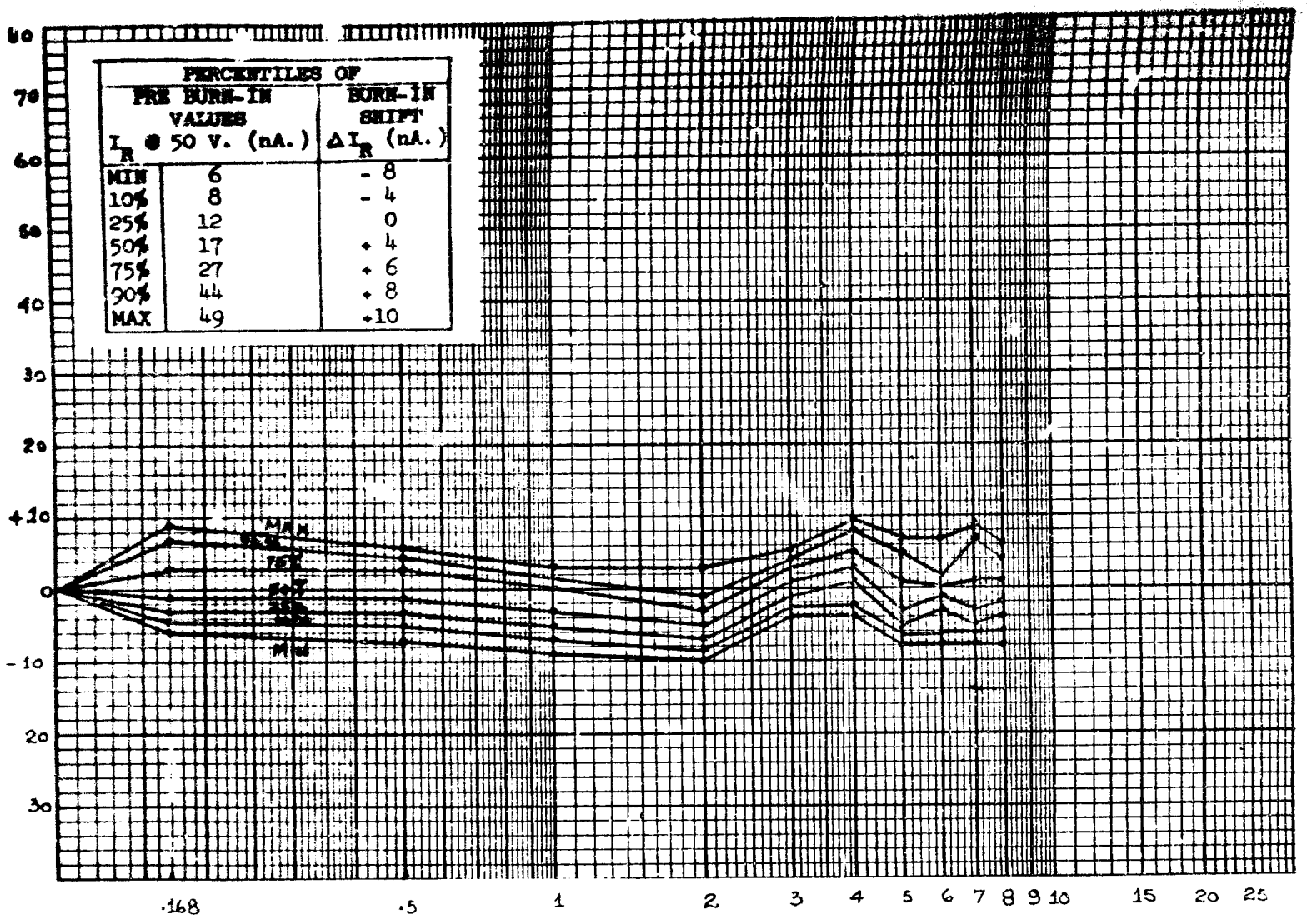


FIGURE 50-4

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 mA. AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: C
SAMPLE SIZE: 2c

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	7	-10
10%	7	-10
25%	7	- 2
50%	12	0
75%	25	+ 2
90%	34	+ 6
MAX	41	+ 7

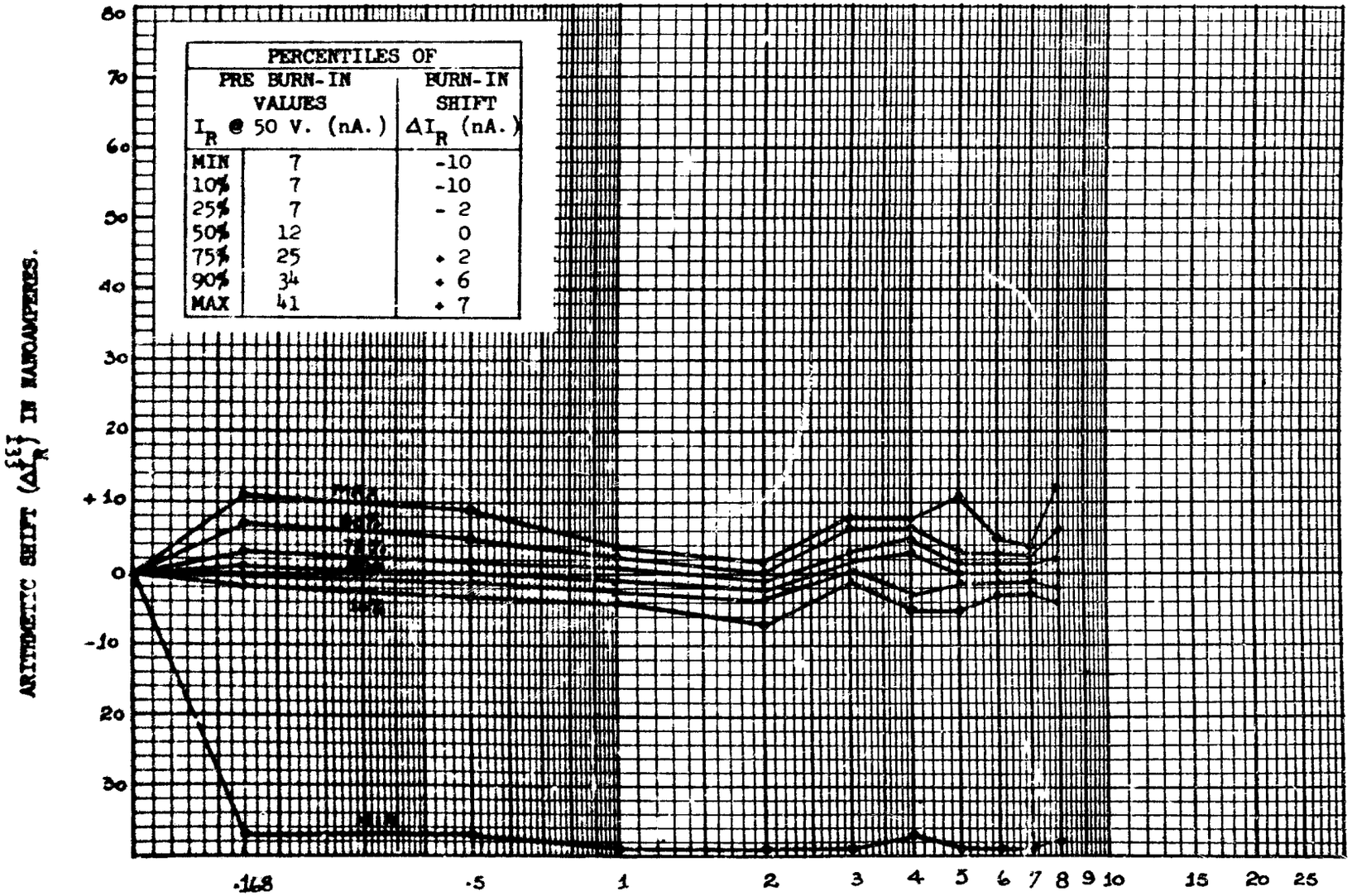
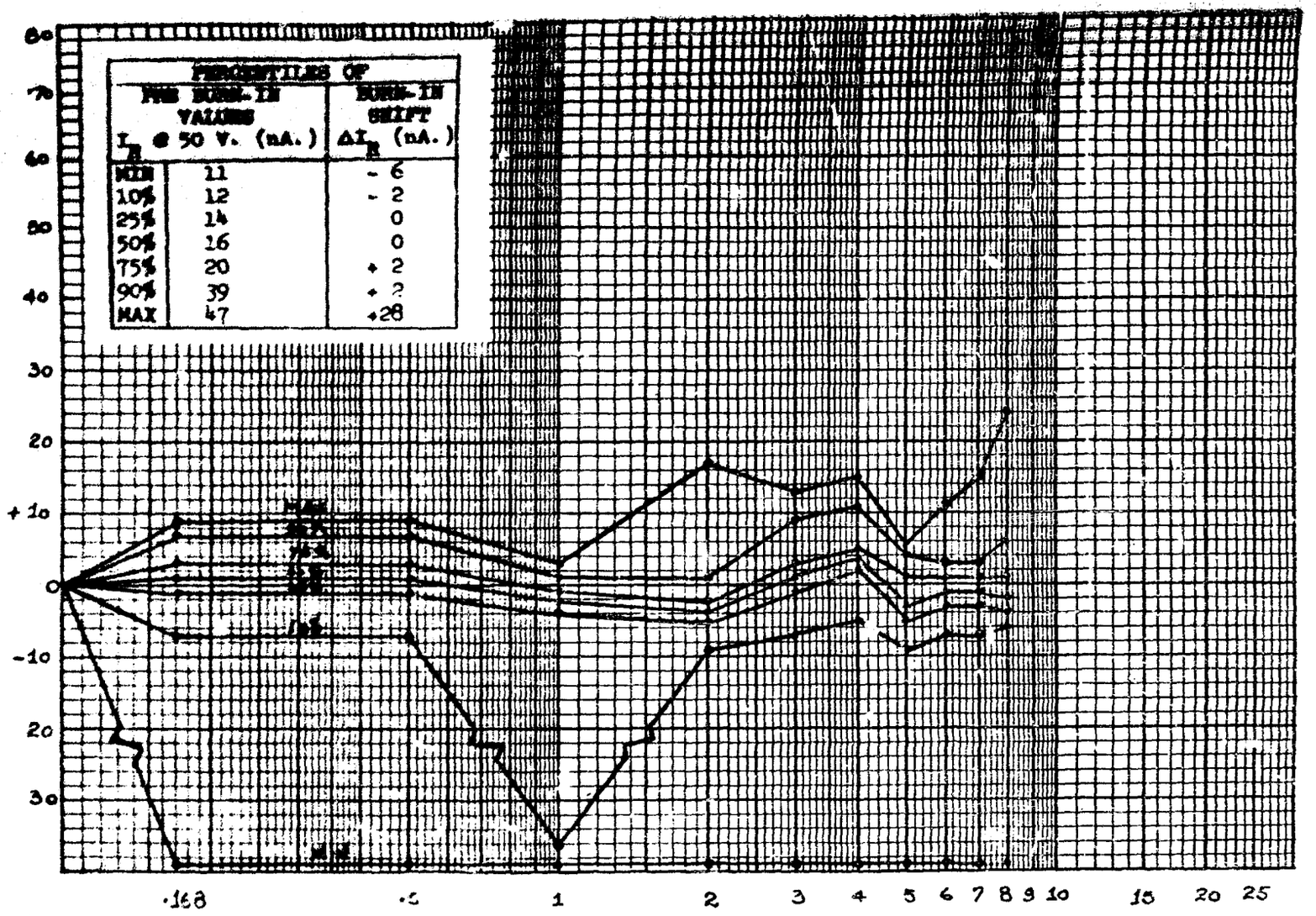


FIGURE 50-5

PERCENTILES OF ARITHMETIC SHIFT OF I_R @ 50 V. FROM BURN-IN VALUES FOR LONG TERM LOW LEVEL FORWARD BIAS TEST AT 50 mA. AT ROOM TEMPERATURE. (STRESS CELL 4).

DIFFUSION LOT: 6
SAMPLE SIZE: 30

PERCENTILES OF	PRE BURN-IN VALUES I_R @ 50 V. (nA.)	BURN-IN SHIFT ΔI_R (nA.)
MIN	11	- 6
10%	12	- 2
25%	14	0
50%	16	0
75%	20	+ 2
90%	39	+ 2
MAX	47	+28



ARITHMETIC SHIFT (ΔI_R) IN NANOAMPERES.

TIME UNDER STRESS IN THOUSANDS OF HOURS.

FIGURE 50-6

REFERENCES

1. F.J. Morin and J.P. Maita, Phys. Rev. 96, 28 (1956).
2. H.C. Gorton, oral presentation, Fourth Annual Symposium on the Physics of Failure in Electronics, Chicago (1965). to be published.
3. D.J. Rose, Phys. Rev., 105, 413 (1957).
4. W. Shockley, Solid State Elect. 2, 35, (1961).
5. R.H. Haitz, J. Appl. Phys. 35, 1370 (1964) and J. Appl. Phys. 36, 3123 (1966).
6. K.S. Champin, J. Appl. Phys. 30, 1039 (1959).
7. R.J. McIntyre, J. Appl. Phys. 32, 983, (1961).
8. J.M. Fairfield and G.H. Schwuttka, J. Appl. Phys. 37, 1536 (1966).
9. Second Technical Documentary Report, February 1966, RADC Contract #AF30-(602)-3624. Pages 22-24.
10. Henning and Miller, Emitter Softening in Diffused Silicon Transistors - 3rd Physics of Failure Symposium, Chicago, September 29, 1964.
11. Poe, Procedures and Observations in Reject Analysis of Surface Degraded Transistors, Physics of Failure Symposium, Rome, New York - April 20,1965
12. Kang, Detailed Study of Deleterious Effects on Silicon Transistors, Technical Documentary Report,- TDR-64-436, December 64.
13. Goetzberger and Shockley, Metal Precipitates in Silicon P-N Junctions, J. Appl Phys. 31, 1821 (October 1960).

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY (Corporate author)
General Electric Company
Semiconductor Products Dept.
Electronics Park; Syracuse, New York 13201

2a REPORT SECURITY CLASSIFICATION
UNCLASSIFIED

2b GROUP

3 REPORT TITLE

Failure Mechanisms in Semiconductor Diodes

4 DESCRIPTIVE NOTES (Type of report and inclusive dates)
Semi-annual - 4 Jan 66 to 3 Jul 66

5 AUTHOR(S) (Last name, first name, initial)

Bair, Byron L.

6 REPORT DATE	7a TOTAL NO OF PAGES	7b NO OF REFS
October 1966	154	13

8a CONTRACT OR GRANT NO.	9a ORIGINATOR'S REPORT NUMBER(S)
AF30(602)-3624	
b PROJECT NO 5519	
c Task No. 551906	9b OTHER REPORT NO(S) (Any other numbers that may be assigned this report) RADC-TR-66-505
d System No. 760K	

10 AVAILABILITY/LIMITATION NOTICES
This document is subject to special export controls and each transmittal to foreign governments or foreign nationals may be made only with prior approval of RADC (EMLI), Griffiss AFB NY 13440.

11 SUPPLEMENTARY NOTES	12 SPONSORING MILITARY ACTIVITY
	Rome Air Development Center (EMEEP) Griffiss Air Force Base, New York 13440

13 ABSTRACT

This is the third semi-annual report of a three year program to investigate those mechanisms which contribute to the long term degradation of diode parameters. This report is primarily concerned with the structuring, refining and verification of a Deterministic Model for diode failure. The Deterministic Model is presently separated into two portions; reverse bias degradation and forward bias degradation.

The reverse bias portion of the model was derived and discussed in the second Technical Documentary Report. This portion of the model is repeated in this report, which also contains:

- sample degradation rate constant calculations,
- a discussion of the preliminary verification of the model,
- the planned test matrix to complete the verification and refinement of the model,
- a summary of the failure analysis effort performed to structure and verify this portion of the model.

See continuation sheet.

DD FORM 1473

UNCLASSIFIED

Security Classification

Security Classification

KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Failure Mechanisms Reliability Semiconductor Diodes						

INSTRUCTIONS

1. ORIGINATING ACTIVITY: Enter the name and address of the contractor, subcontractor, grantee, Department of Defense activity or other organization *(corporate author)* issuing the report.

2a. REPORT SECURITY CLASSIFICATION: Enter the overall security classification of the report. *Indicate* whether "Restricted Data" is included. Marking is to be in accordance with appropriate security regulations.

2b. GROUP: Automatic downgrading is specified in DoD Directive 5200.10 and Armed Forces Industrial Manual. Enter the group number. Also, when applicable, show that optional markings have been used for Group 3 and Group 4 as authorized.

3. REPORT TITLE: Enter the complete report title in all capital letters. Titles in all cases should be unclassified. If a meaningful title cannot be selected without classification, show title classification in all capitals in parenthesis immediately following the title.

4. DESCRIPTIVE NOTES: If appropriate, enter the type of report, e.g., interim, progress, summary, annual, or final. Give the inclusive dates when a specific reporting period is covered.

5. AUTHOR(S): Enter the name(s) of author(s) as shown on or in the report. Enter last name, first name, middle initial. If military, show rank and branch of service. The name of the principal author is an absolute minimum requirement.

6. REPORT DATE: Enter the date of the report as day, month, year, or month, year. If more than one date appears on the report, use date of publication.

7a. TOTAL NUMBER OF PAGES: The total page count should follow normal pagination procedures, i.e., enter the number of pages containing information.

7b. NUMBER OF REFERENCES: Enter the total number of references cited in the report.

8a. CONTRACT OR GRANT NUMBER: If appropriate, enter the applicable number of the contract or grant under which the report was written.

8b, 8c, & 8d. PROJECT NUMBER: Enter the appropriate military department identification, such as project number, subproject number, system numbers, task number, etc.

9a. ORIGINATOR'S REPORT NUMBER(S): Enter the official report number by which the document will be identified and controlled by the originating activity. This number must be unique to this report.

9b. OTHER REPORT NUMBER(S): If the report has been assigned any other report numbers *(either by the originator or by the sponsor)*, also enter this number(s).

10. AVAILABILITY/LIMITATION NOTICES: Enter any limitations on further dissemination of the report, other than those imposed by security classification, using standard statements such as:

(1) "Qualified requesters may obtain copies of this report from DDC."

(2) "Foreign announcement and dissemination of this report by DDC is not authorized."

(3) "U. S. Government agencies may obtain copies of this report directly from DDC. Other qualified DDC users shall request through _____."

(4) "U. S. military agencies may obtain copies of this report directly from DDC. Other qualified users shall request through _____."

(5) "All distribution of this report is controlled. Qualified DDC users shall request through _____."

If the report has been furnished to the Office of Technical Services, Department of Commerce, for sale to the public, indicate this fact and enter the price, if known.

11. SUPPLEMENTARY NOTES: Use for additional explanatory notes.

12. SPONSORING MILITARY ACTIVITY: Enter the name of the departmental project office or laboratory sponsoring *(paying for)* the research and development. Include address.

13. ABSTRACT: Enter an abstract giving a brief and factual summary of the document indicative of the report, even though it may also appear elsewhere in the body of the technical report. If additional space is required, a continuation sheet shall be attached.

It is highly desirable that the abstract of classified reports be unclassified. Each paragraph of the abstract shall end with an indication of the military security classification of the information in the paragraph, represented as *(TS)*, *(S)*, *(C)*, or *(U)*.

There is no limitation on the length of the abstract. However, the suggested length is from 150 to 225 words.

14. KEY WORDS: Key words are technically meaningful terms or short phrases that characterize a report and may be used as index entries for cataloging the report. Key words must be selected so that no security classification is required. Identifiers, such as equipment model designation, trade name, military project code name, geographic location, may be used as key words but will be followed by an indication of technical context. The assignment of links, rules, and weights is optional.

The forward bias portion of the model has proved to be more complex than the reverse bias portion. The observed response to stress has been multi-modal and dependent on the measurement bias voltages. This portion of the model is being structured, but the following points have been determined, and are discussed in this report:

- the temperature and pressure used in the sealing process have a major effect in the degradation response pattern,
- the degradation patterns following the sealing process, forward current stresses and at very high temperature stress at zero bias are identical,
- the degraded devices, which had been stressed in the sealing process, exhibited microplasma light emission, low amplitude microplasma noise pulses and reverse voltage walkout,
- the observed failure mechanisms seem to be surface, rather than bulk, related phenomena,
- there is evidence to indicate that the model should be based on the high temperature decomposition of a compound into components, at least one of which is active in increasing the surface electron concentration,
- the planned test matrix to complete the structuring, verification and refinement of the model,
- a summary of the failure analysis effort performed to date on this portion of the model.

Failure analysis will become an even more important part of the work effort to achieve the objectives of the program. This report contains an explanation of the physical nature of the failure mechanism and a complete Failure Mode Chart which defines codes and related the failure mode categories, failure mechanisms and failure causes.

The comprehensive step-stress tests have been continued. The 175°C forward current, forward voltage and reverse voltage stresses are completed, and the data analyzed. The 200°C and 225°C stresses will be completed next. The step-stress data will be used to extend the range of the reverse bias portion of the Deterministic Model as well as to make certain that all the necessary stresses are included in the Deterministic Model test plan.